Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

ELECTRONICS – ET1

P.M. MONDAY, 12 May 2014

1 hour 15 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**8**	
2.	**6**	
3.	**9**	
4.	**7**	
5.	**6**	
6.	**5**	
7.	**7**	
8.	**12**	
Total	**60**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES IN ET1

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B+1) = A$$

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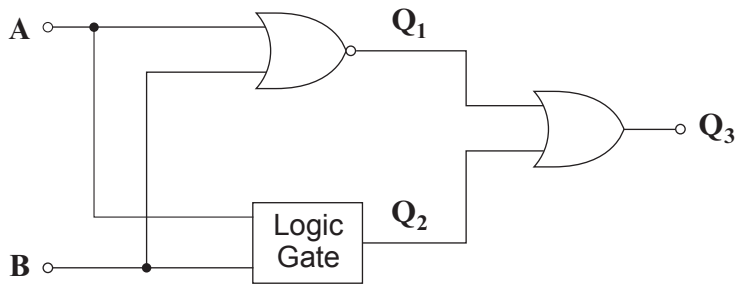
Examiner only

1. The following diagram shows a logic system.



(a) The partially completed truth table for the logic system is shown below.

INPUTS		OUTPUTS		
B	**A**	Q_1	Q_2	Q_3
0	0		0	
0	1		1	
1	0		1	
1	1		0	

(i) Identify the logic gate that gives output Q_2. [1]

Gate .....

(ii) Complete the truth table for the outputs Q_1 and Q_3. [2]

(b) Give the Boolean expression for **each** of the outputs Q_1, Q_2 and Q_3 in terms of **A** and **B**. [3]

Q_1 = ...

Q_2 = ...

Q_3 = ...

(c) Name the single gate that would produce the same output as Q_3. [1]

.....

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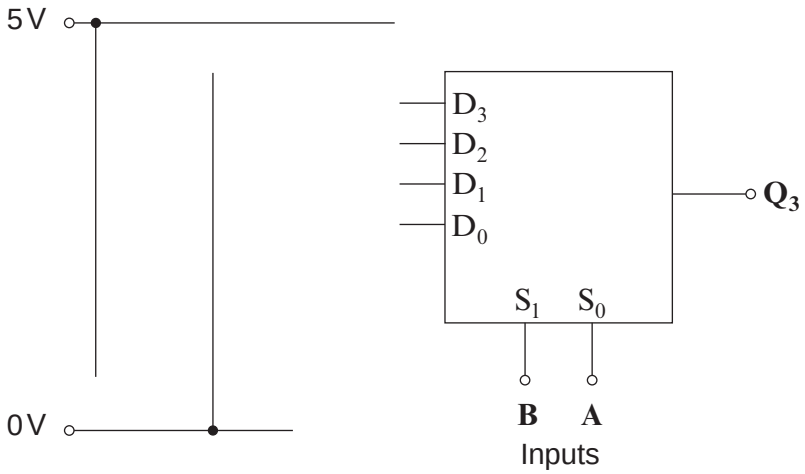
(d) Show on the following diagram how the same output $\mathbf{Q_3}$ could be generated using a multiplexer. [1]



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2. The truth table for a logic gate is given below.

B	A	Q
0	0	1
0	1	0
1	0	0
1	1	1

(a) Using only AND, OR and NOT gates, draw a diagram of a logic system that will produce this truth table. [1]

(b) Redraw your system in part *(a)* using only NAND gates. [3]

(c) Draw lines through all redundant gates. [2]

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3. *(a)* Simplify the following expressions, showing your working where appropriate.

(i) $\bar{A}.1$ = ... [1]

(ii) $(B + \bar{A}).(\bar{B} + A)$ = ...

..... [2]

(b) A different logic system produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show any groups that you create on the map. [3]

.....

.....

.....

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result.
All steps of the simplification must be shown. [3]

$$Q = \overline{(\bar{A}.\bar{B}).(A + \bar{B})}$$

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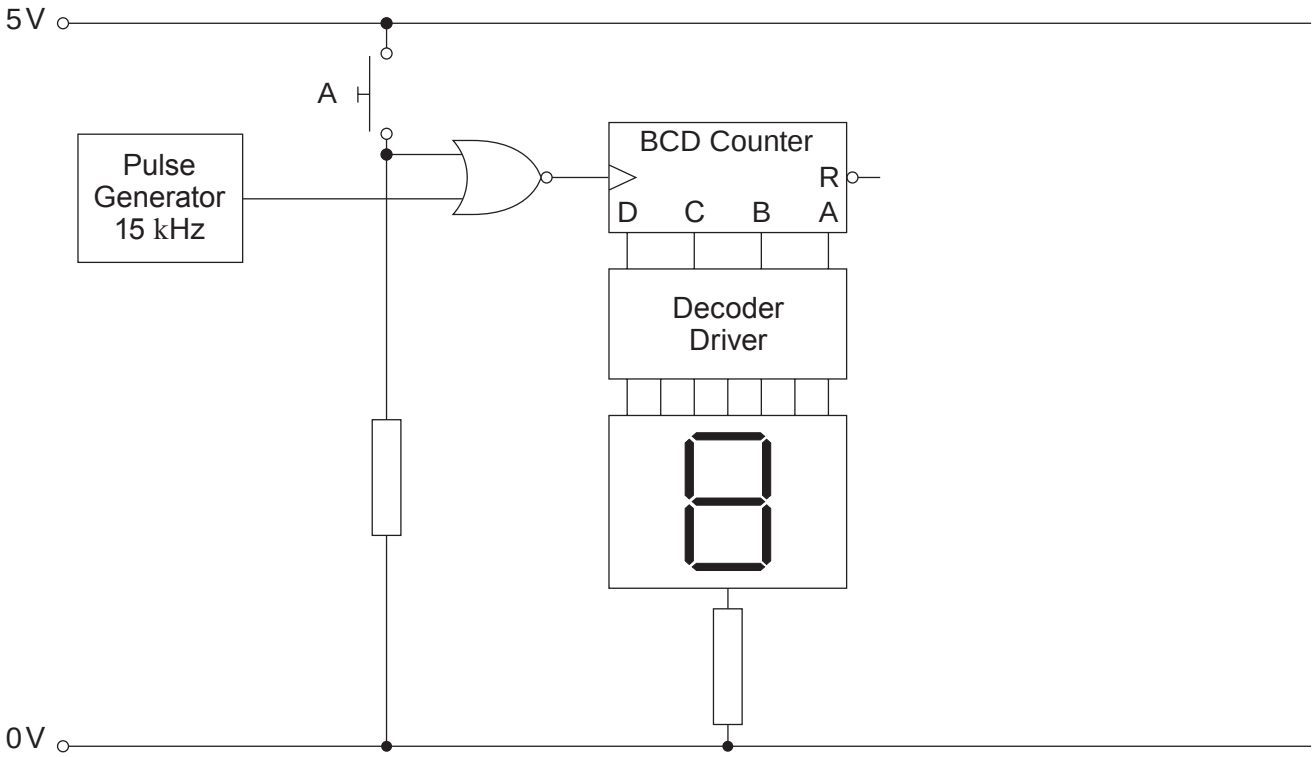
4. The incomplete circuit diagram shows a simple random number generator.



(a) (i) What does the circle (○) on the reset connection indicate? [1]

.....

(ii) **Complete** the circuit diagram by adding a logic gate and suitable connections so that the largest number displayed is 5. [3]

(b) Describe, in detail, what happens to the display when:

(i) switch A is open; [1]

.....

.....

(ii) switch A is pressed and held closed. [1]

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.....

(c) Explain why a 15 kHz astable is suitable for this application. [1]

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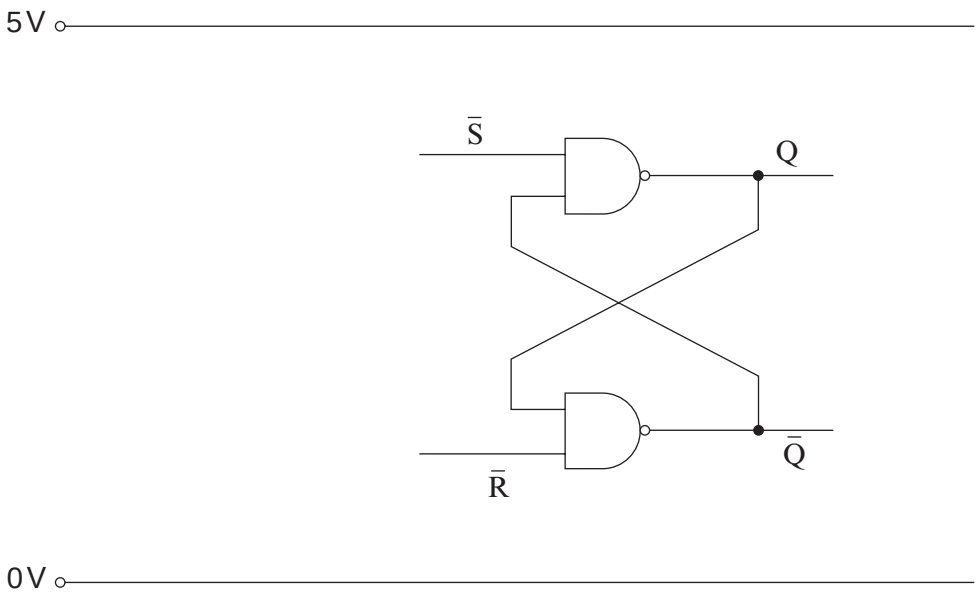
5. The circuit diagram shows one part of an alarm system.



(a) Inputs $\bar{S}$ and $\bar{R}$ are operated in the following sequence. Complete the truth table to show how the outputs Q and $\bar{Q}$ respond. [2]

$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
1	1	0	
0	1		
1	1		
1	0		
1	1		

(b) Add the necessary components to the diagram such that the $\bar{S}$ input can be used to **set** Q to logic 1 when a switch is momentarily pressed. [2]

(c) The output of the alarm is a LED.
Complete the diagram to show how the LED can be used to indicate the logic state of $\bar{Q}$.
The LED should be ON when $\bar{Q}$ is **sinking a current**. [2]

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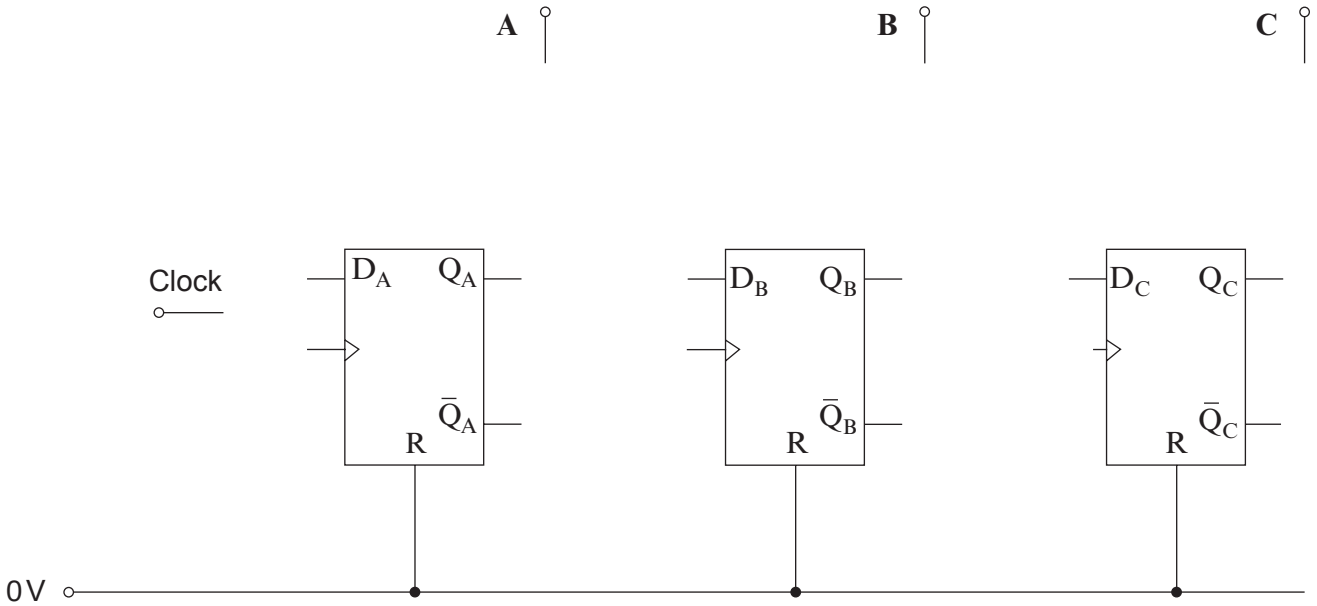
6. The diagram shows 3 D-type flip-flops, which form part of a binary **down-counter**. Outputs **A**, **B** and **C** are used to indicate the binary output. **A** is the **least significant bit**.



(a) Complete the diagram to make a three bit binary **down-counter**. [3]

(b) The initial state of the counter is shown in the table. Complete the table, using **0** or **1**, to indicate the logic state of **each** output after the stated number of clock pulses. [2]

	OUTPUT C	**OUTPUT B**	**OUTPUT A**
Initial State	1	1	1
After ONE clock pulse			
After SIX clock pulses			

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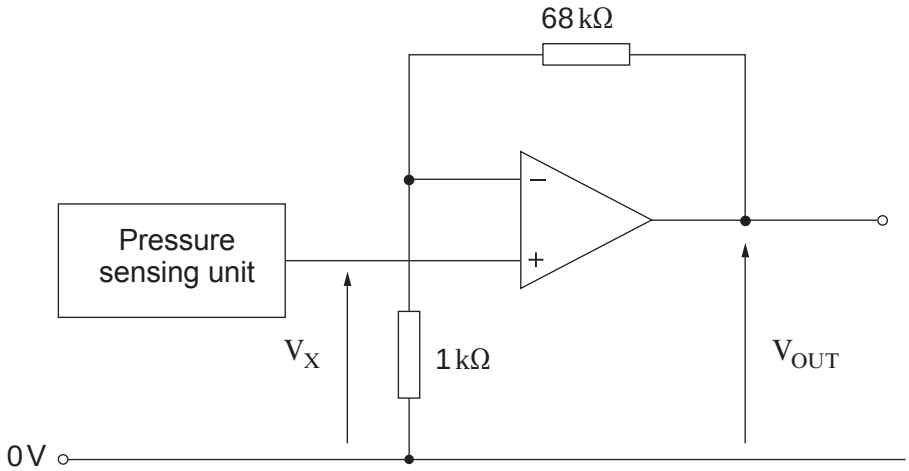
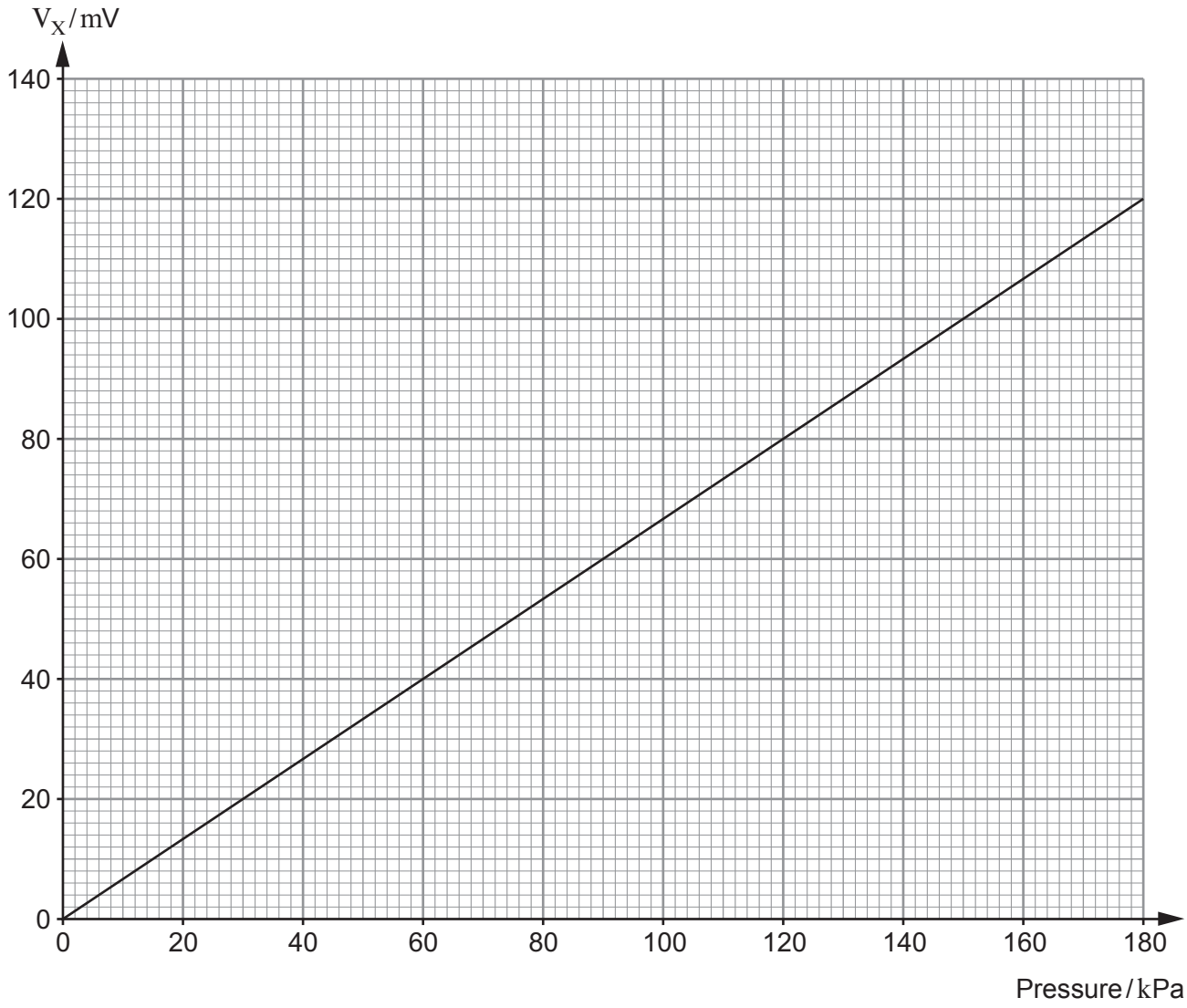
7. The circuit diagram shows part of a diver's pressure gauge system. The output of the pressure sensing unit is amplified using a voltage amplifier based on an op-amp.



The calibration graph for the pressure sensing unit is shown below. Pressure is measured in units called kPa.



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(a) What is the voltage gain of the amplifier? [1]

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.....

(b) Use the calibration graph to:

(i) determine the pressure when $V_X = 90\ mV$;

.....

(ii) calculate the output voltage V_{OUT} of the amplifier at 110 kPa. [3]

.....

.....

(c) The op-amp saturates at $\pm 8.0\,V$. Determine the **maximum** pressure that this system can measure. [3]

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Turn over.

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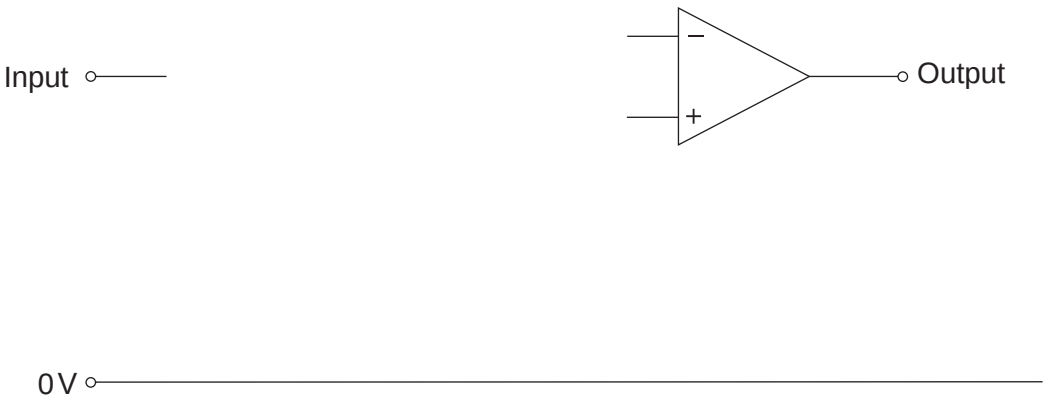
8. A data sheet for an op-amp is given below.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12} \Omega$
Saturation voltage for a ± 13 V supply	± 12 V
Slew rate	$4.8\ \text{V}\ \mu\text{s}^{-1}$
Gain-bandwidth product	3.6 MHz

The op-amp is powered from a ± 13 V supply.

An amplifier has a **variable** voltage gain. The minimum voltage gain is 0 and the maximum voltage gain is – 60.

(a) Complete the circuit diagram for a voltage amplifier with this specification. [3]



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(b) (i) Calculate the **two** resistance values which give a maximum voltage gain of –60. Identify the feedback resistance. [2]

.....

.....

(ii) What is the input impedance of this voltage amplifier? [1]

.....

(c) The voltage gain is adjusted and the output voltage measured to be –9 V when the input voltage is 200 mV. Calculate the new voltage gain. [1]

.....

.....

(d) The voltage gain is changed to –30. Calculate the maximum bandwidth of the amplifier with this voltage gain. [2]

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TURN OVER FOR THE REST OF THE QUESTION.

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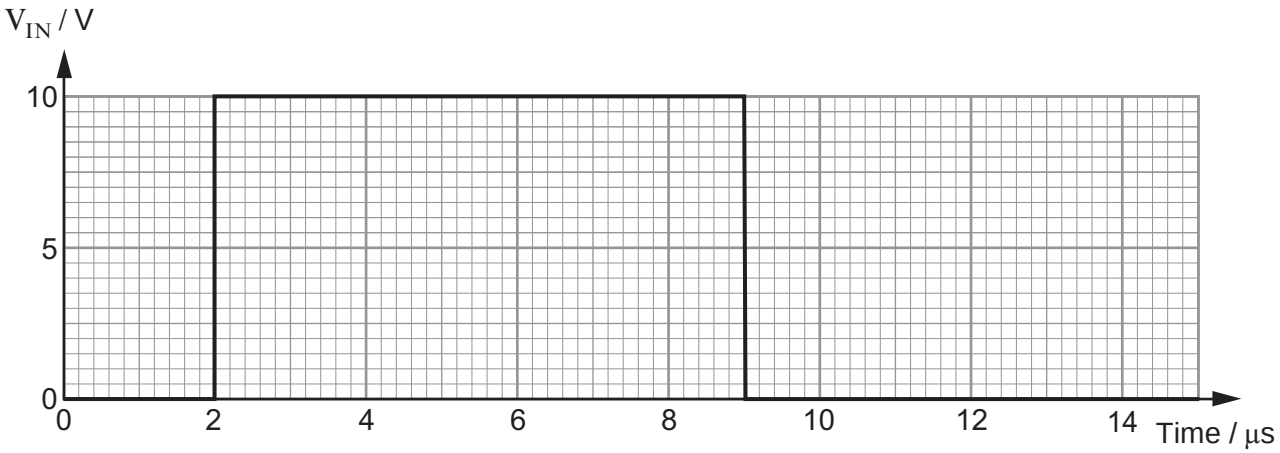
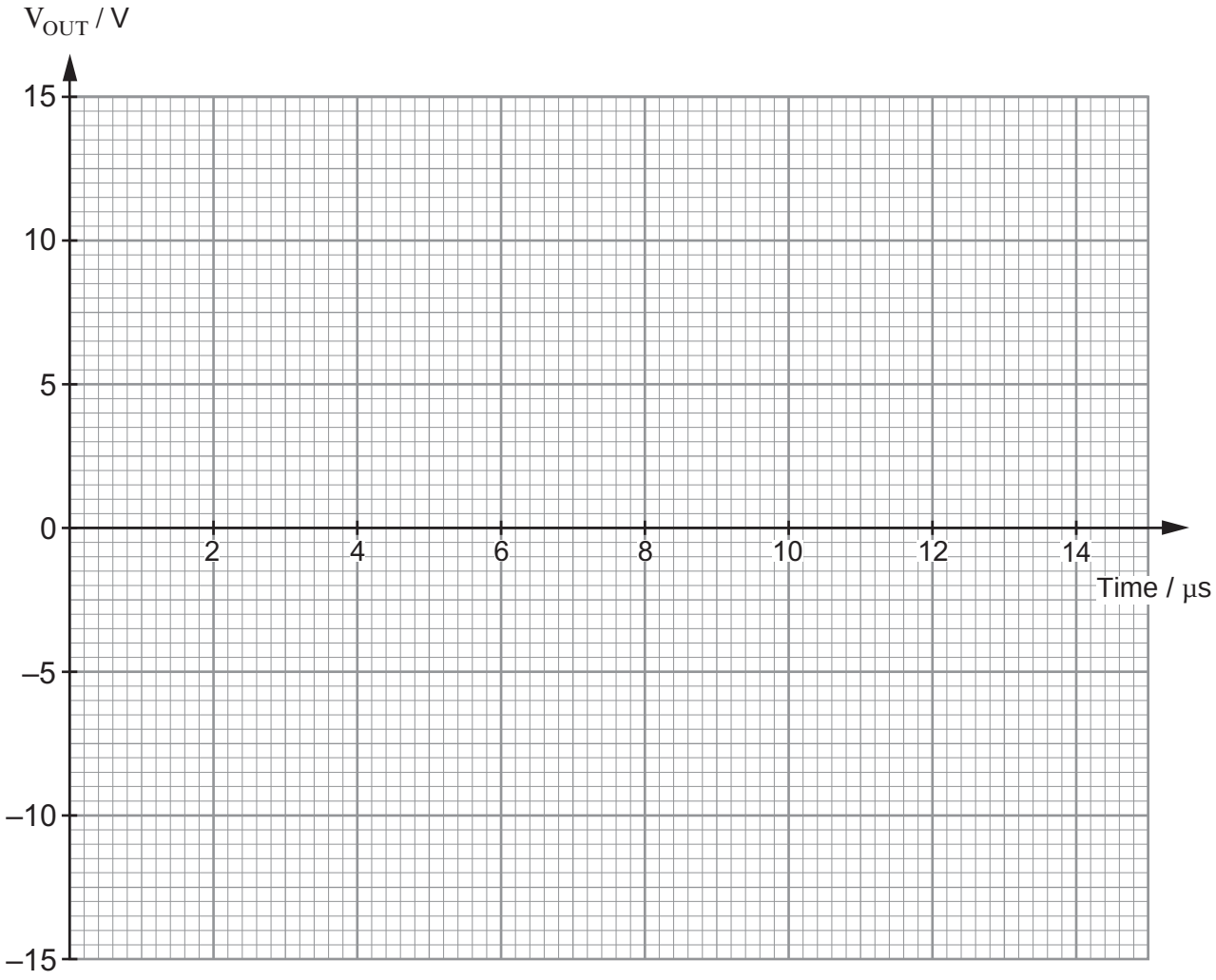
(e) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.

Draw the output voltage on the axes below. **V_{OUT} is initially at 0 V.** [3]





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