Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

ELECTRONICS – ET1

A.M. MONDAY, 20 January 2014

1 hour 15 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**4**	
2.	**8**	
3.	**4**	
4.	**9**	
5.	**6**	
6.	**6**	
7.	**4**	
8.	**12**	
9.	**7**	
Total	**60**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES IN ET1

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B+1) = A$$

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1. *(a)* What type of 2-input logic gate:

(i) outputs a logic 1 only when both inputs are at logic 1? ..... [1]

(ii) outputs a logic 1 only when both inputs are at logic 0? ..... [1]

(b) The truth table for a logic gate is shown below.

B	A	Q
0	0	0
0	1	1
1	0	1
1	1	0

(i) What logic gate produces this truth table?

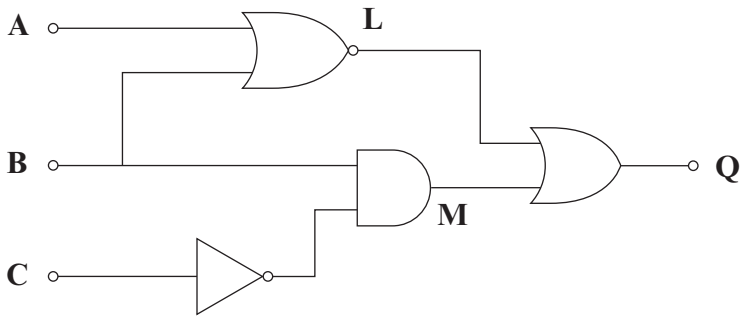
.....

(ii) Draw the circuit symbol for this logic gate.

[2]

Examiner only

2. *(a)* The following diagram shows a logic system.



Write down Boolean expressions for the outputs **L**, **M** and **Q** in terms of inputs **A**, **B** and **C**. [3]

L = ...

M = ...

Q = ...

(b) (i) Redraw the logic system replacing each gate with its NAND gate equivalent. [3]

(ii) Draw lines through all redundant gates. [2]

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3. Some modern cars have systems to switch on windscreen wipers either automatically when moisture is detected or when they are switched on manually by the driver. The system only operates if the ignition switch is on.

- Wiper switch **C** outputs a logic 1 when it is switched on by the driver.
- Moisture sensor **B** outputs a logic 1 when rain is detected.
- Ignition switch **A** outputs a logic 1 when it is switched on.
- The windscreen wiper motor operates when output **Q** is at logic 1.

(a) Complete the truth table for the logic system. [1]

Wiper switch **C**	Moisture sensor **B**	Ignition switch **A**	Wiper motor **Q**
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(b) Write down the Boolean expression for **Q** in terms of **C**, **B** and **A**.
There is no need to simplify it.

Q = ... [2]

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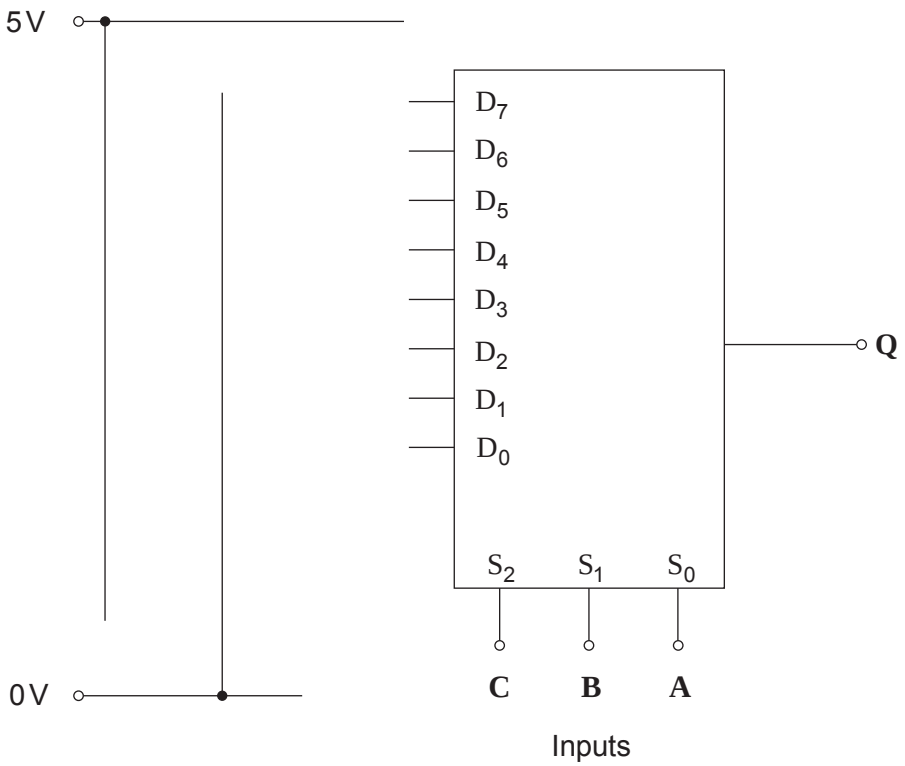
(c) Show on the following diagram how the same output as **Q** can be generated using an 8 to 1 multiplexer. [1]



Turn over.

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4. *(a)* Simplify the following Boolean expressions. [2]

(i) $A + 1 =$ .....

(ii) $\overline{C}.D + C =$ .....

(b) Using either a Karnaugh map or the rules of Boolean algebra simplify the following expression as much as possible. [4]

$Q = D.C.A + \overline{D}.C.B.A + \overline{C}.\overline{B}.\overline{A} + C.\overline{B}.A. + D.C.B$

DC \ BA	00	01	11	10
00				
01				
11				
10				

.....

.....

.....

.....

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. [3]

$$Q = \overline{\overline{(A + \overline{B})} + \overline{B}}$$

.....

.....

.....

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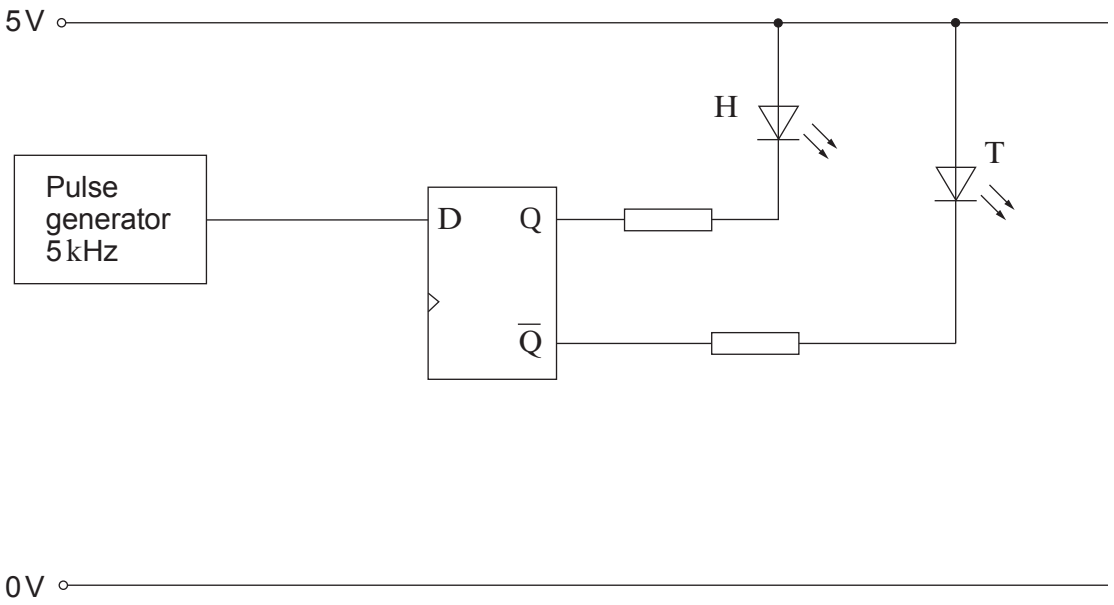
5. The diagram shows an incomplete circuit for an electronic *coin-tossing* game in which LED H represents *Heads* and LED T represents *Tails*.

The D-type flip-flop is *rising-edge-triggered*.



(a) Add the necessary components to the diagram to produce a *rising-edge* at the clock input when a switch is pressed. [2]

(b) What is the logic state of $\overline{Q}$ when LED T is on? [1]

Logic state of $\overline{Q}$ = ...

(c) Consider what happens when the clock input rises from logic 0 to logic 1 whilst the output of the pulse generator is high.

(i) What is the resulting logic state of the Q output? [1]

Logic state of Q .....

(ii) Describe the state of **each** of the LEDs using the words **'OFF'** or **'ON'.** [1]

H = ... T = ...

(d) Why is a frequency of 5 kHz suitable for this application? [1]

.....

.....

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Turn over.

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6. All logic gates have a *propagation delay*.

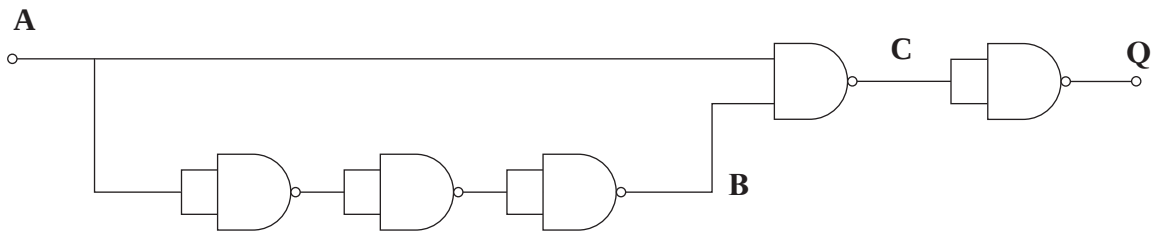
(a) What is meant by *propagation delay*? [1]

.....

.....

(b) A simple transition gate makes use of this propagation delay.

For each logic gate the propagation delay is 10 ns.



The signal, shown on the graph opposite is applied to input **A**.

Show on the graph how the logic levels at **B**, **C** and **Q** change over the course of 80 ns. [5]

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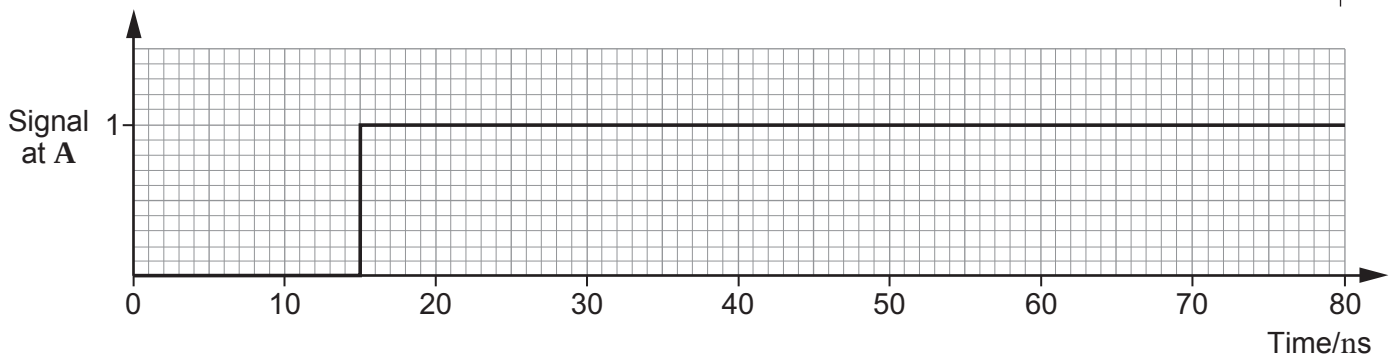

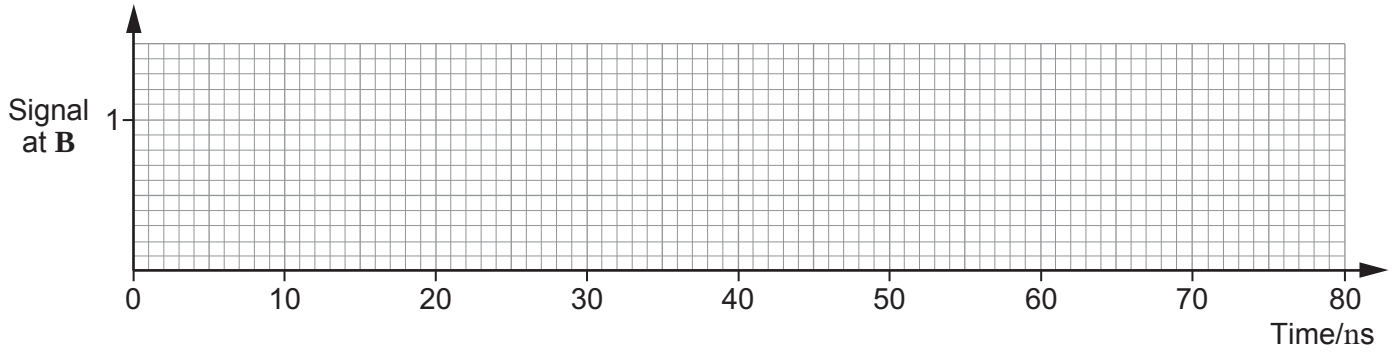

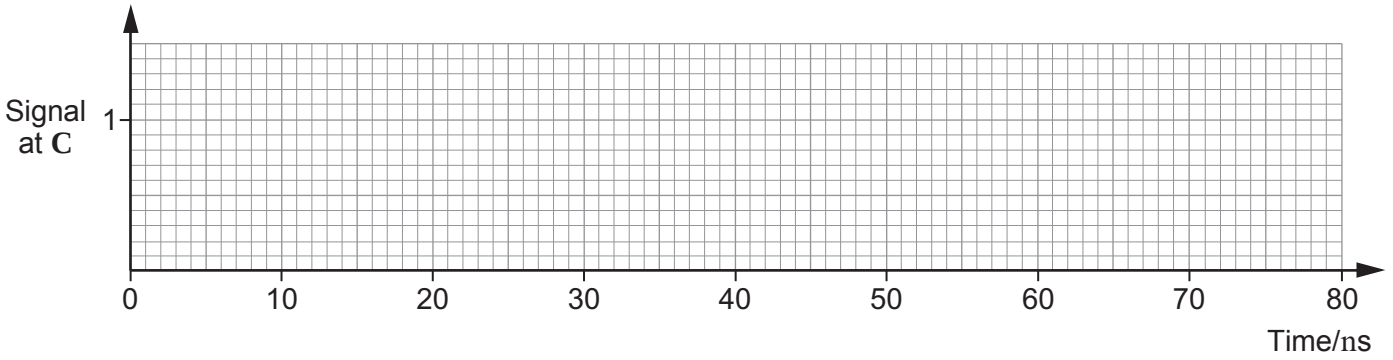

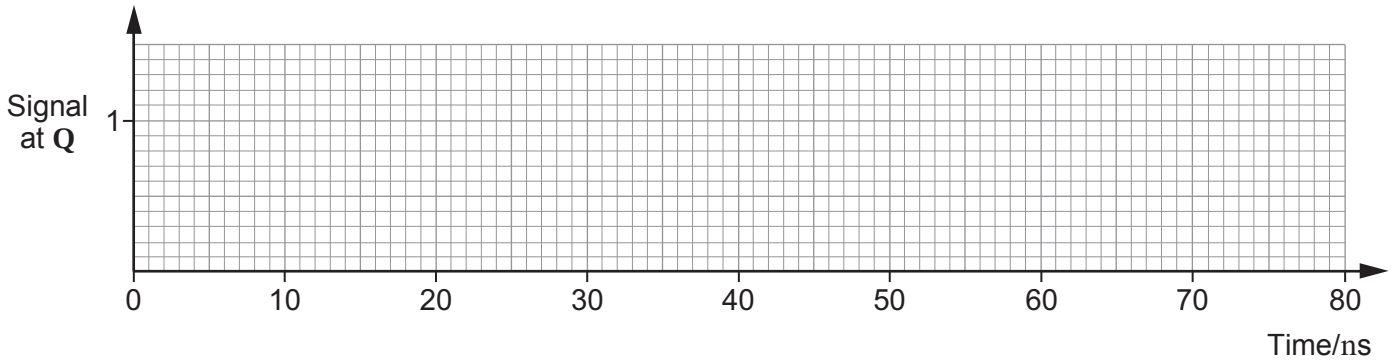

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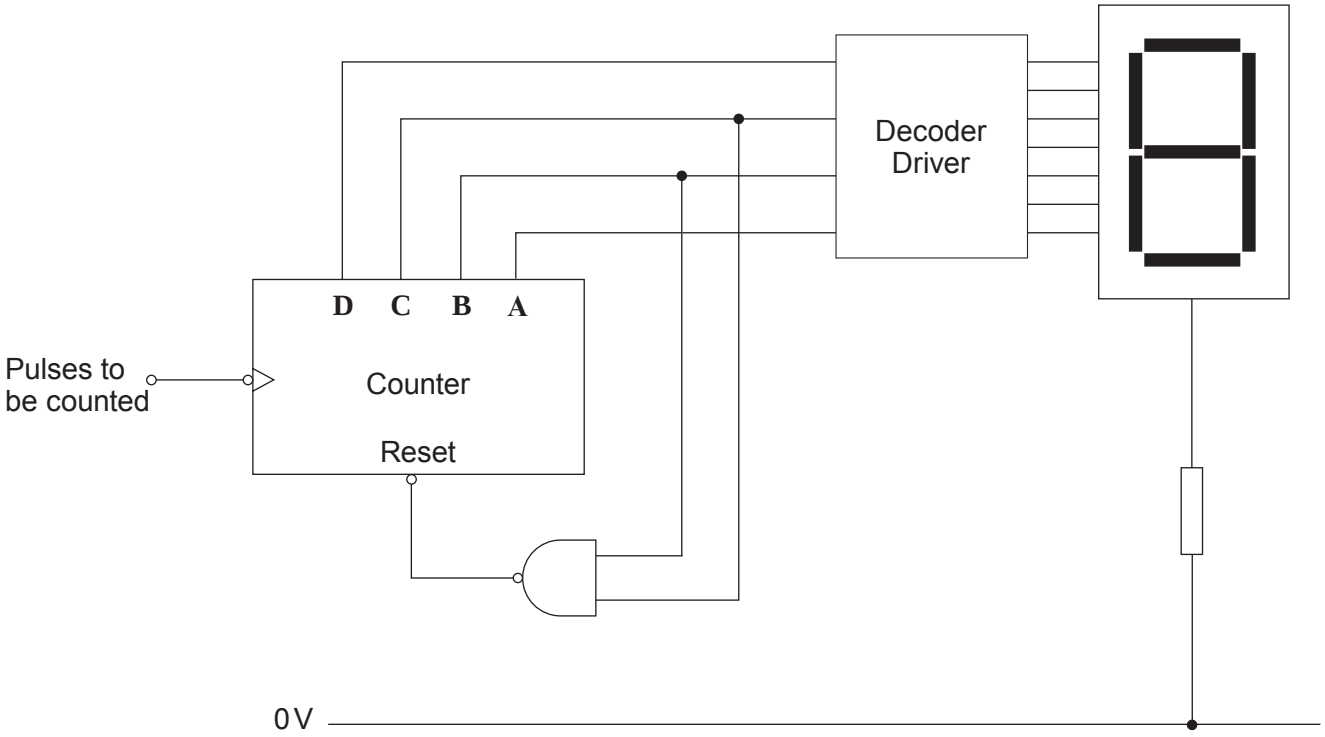
7. The diagram below shows a counting system that uses a 4-bit counter and 7-segment display.

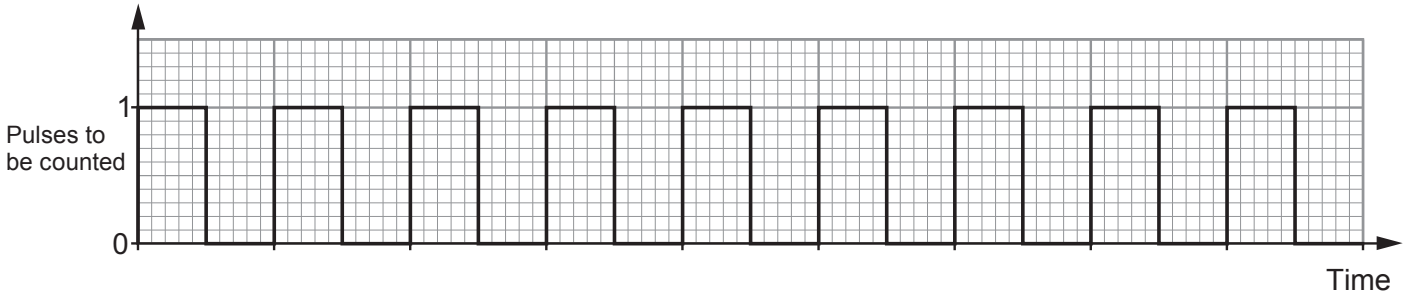


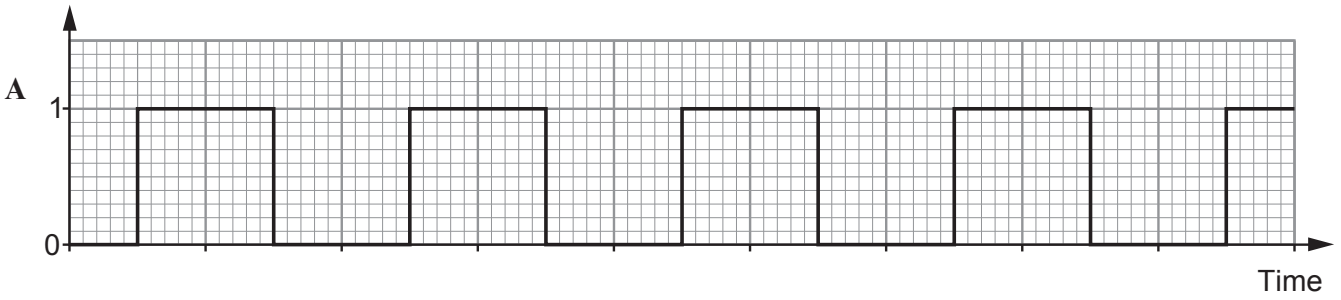
(a) What is the highest number that will be displayed before the counter is reset? [1]

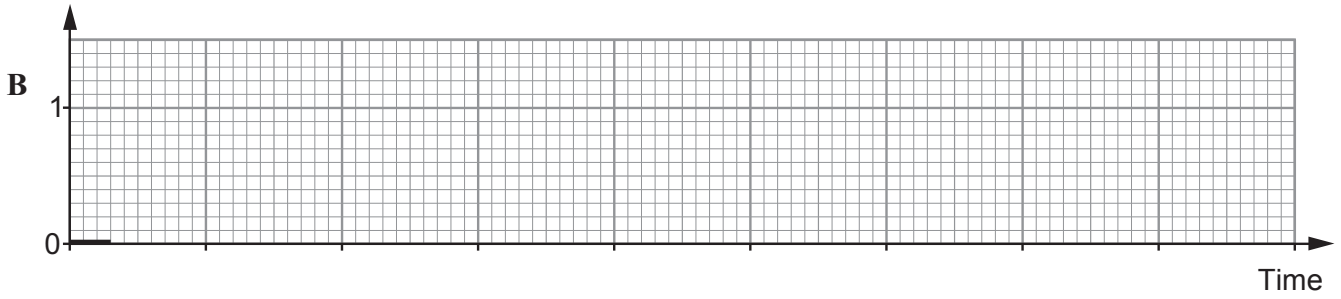
.....

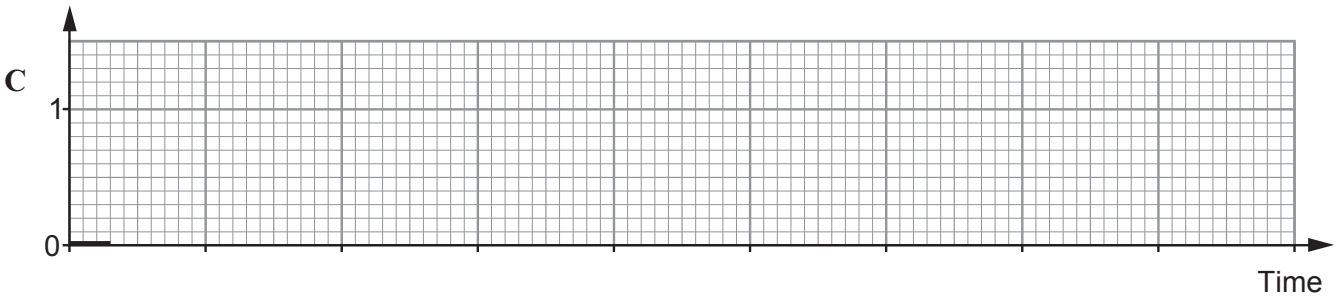
Examiner only

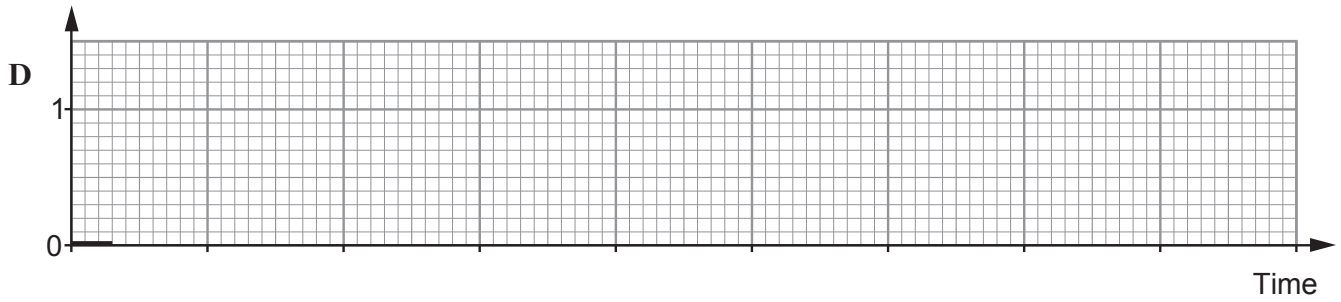
(b) The timing diagram shows pulses to be counted by the system. The counter is *falling-edge* triggered. Complete the graph to show the signals at outputs **B**, **C** and **D**. Initially the counter is reset. [3]











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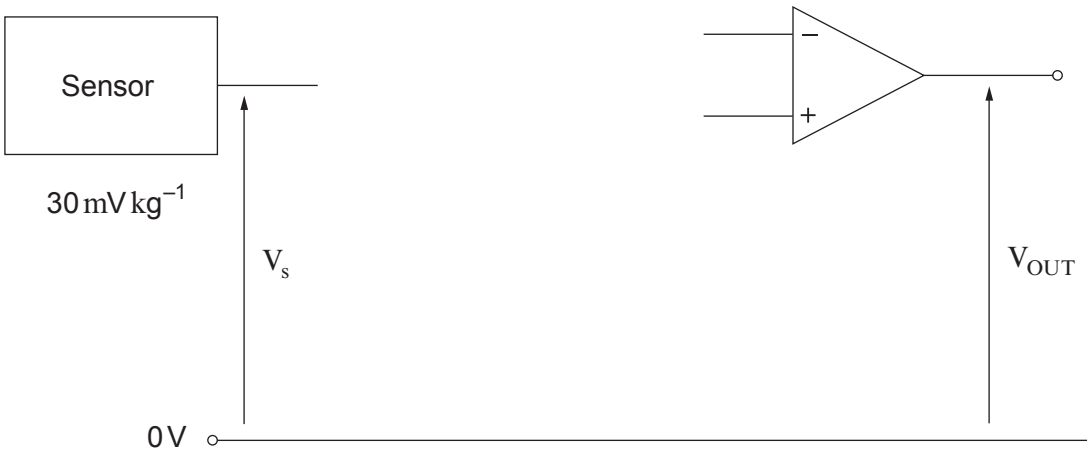
8. An electronic balance uses a sensor connected to a voltage amplifier. The output of the sensor changes by 30 mV for each kg change in mass.

(a) Complete the circuit diagram for a non-inverting amplifier based on an op-amp with the sensor connected to the input. [3]



An engineer tests the calibration of the balance. The table shows how V_{OUT} changes with mass.

mass/kg	V_{OUT}/V
0	0
1	1.2
2	2.4
3	3.8
4	4.8
5	6.0
6	7.0
7	8.4
8	8.8
9	8.8
10	8.8

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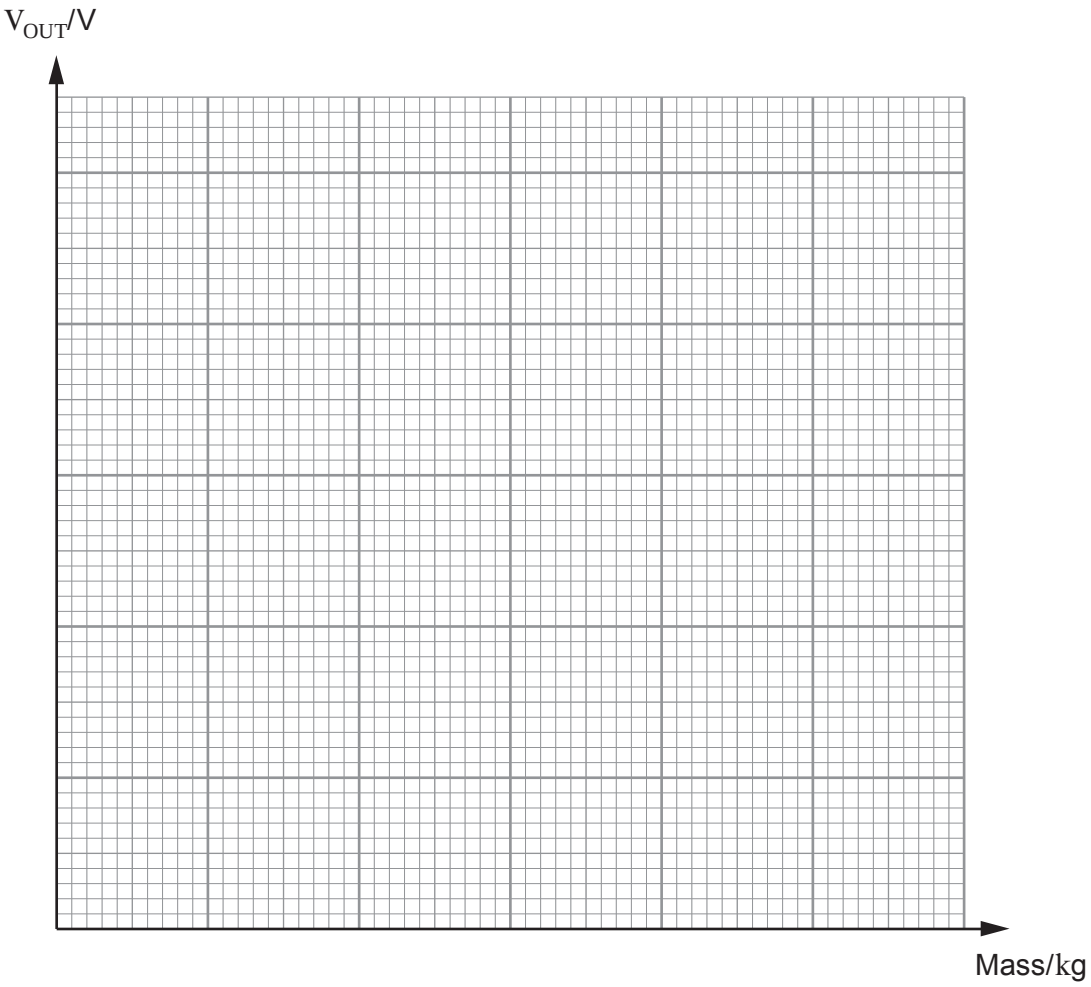
(b) Choose a suitable scale for the axes and plot the graph of V_{OUT} against mass for these results. [3]



(c) Use the graph to deduce:

(i) the saturation voltage; [1]

.....

(ii) the output voltage when the mass is 4.2 kg; [1]

.....

(iii) the maximum mass the balance can accurately register. [1]

.....

(d) (i) Calculate the input voltage to the amplifier when the mass is 5 kg. [1]

.....

(ii) Hence calculate the voltage gain of the amplifier. [2]

.....

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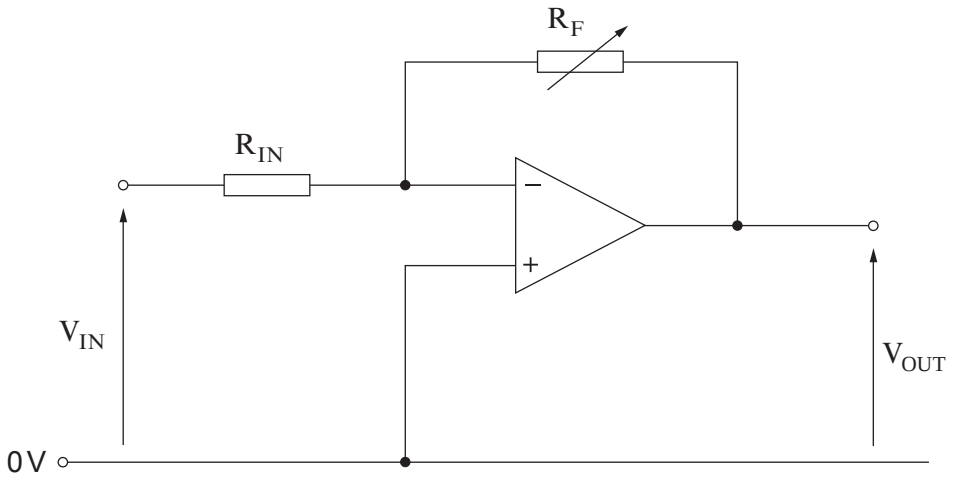
9. An extract from the data sheet for an op-amp is given below.

The op-amp is powered from a ± 16 V supply.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12} \Omega$
Saturation voltage	± 15.0 V
Slew rate	$6.25\ V\,\mu s^{-1}$
Gain-bandwidth product	3.2 MHz

The diagram shows the op-amp used in a voltage amplifier circuit. The variable resistor allows the user to change the gain.



The input signal was set to amplitude 5 mV. The variable resistor was adjusted to give the output signal shown on the next page.

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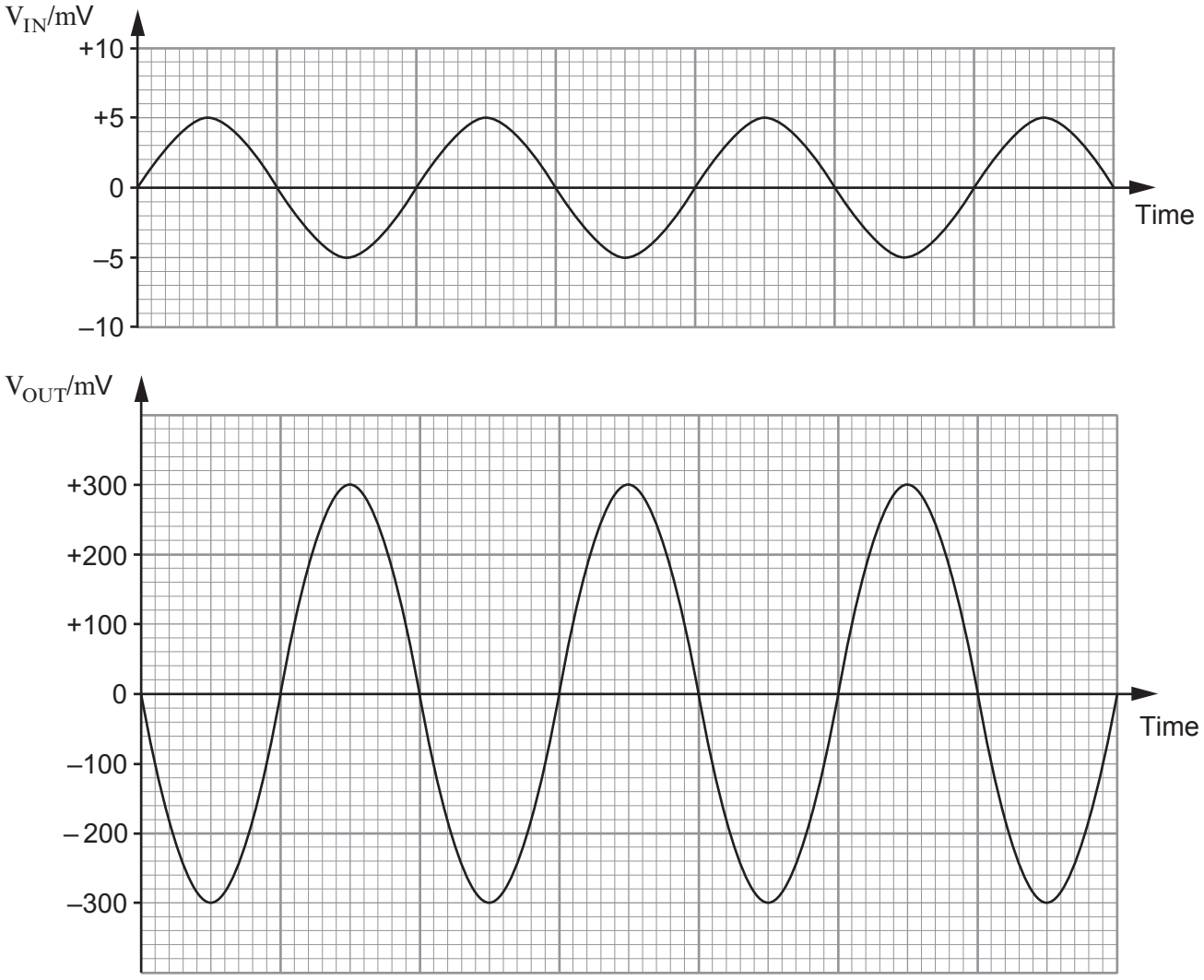

(a) (i) Determine the voltage gain of the amplifier. [1]

.....

.....

(ii) Select suitable values for the input resistor and the resistance setting of the variable resistor, R_F. [2]

R_{IN} .....

R_F .....

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(b) The variable resistor was adjusted to give a voltage gain of – 40. Calculate the bandwidth of the amplifier for this value of voltage gain. [2]

.....

.....

(c) In response to a step change in input the output voltage changes from – 15 V to + 15 V. Calculate the time taken for this change in output voltage to occur. [2]

.....

.....

.....

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END OF PAPER

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