Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A Level

1141/01

S17-1141-01

ELECTRONICS – ET1

TUESDAY, 16 MAY 2017 – AFTERNOON

1 hour 15 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**8**	
2.	**9**	
3.	**7**	
4.	**10**	
5.	**7**	
6.	**8**	
7.	**11**	
Total	**60**	

1141
010001

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier $G = -\dfrac{R_F}{R_{IN}}$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities $A + \overline{A}.B = A + B$

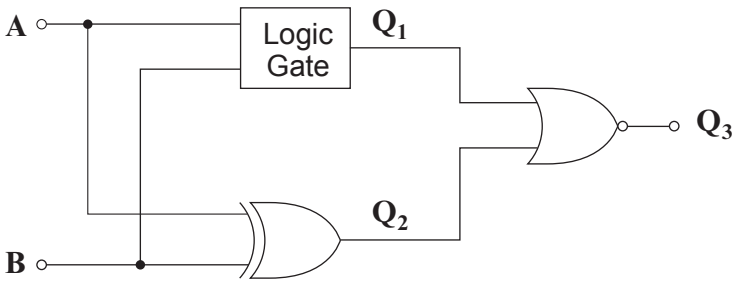
$$A.B + A = A.(B+1) = A$$

BLANK PAGE

Examiner only

Answer **all** *questions.*

1. The following diagram shows a logic system.



(a) The partially completed truth table for the logic system is shown below.

INPUTS		OUTPUTS		
B	**A**	Q_1	Q_2	Q_3
0	0	1		
0	1	1		
1	0	1		
1	1	0		

(i) Identify the logic gate that gives output Q_1. [1]

Gate .....

(ii) **Complete the truth table** for the outputs Q_2 and Q_3. [2]

(b) Give the Boolean expression for each of the outputs Q_1, Q_2 and Q_3 in terms of A and B. [3]

Q_1 = ...

Q_2 = ...

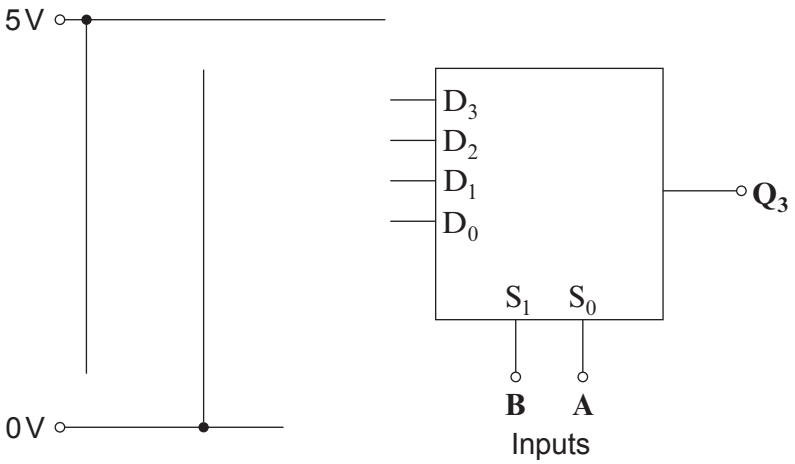
Q_3 = ...

(c) Name the single logic gate that would produce the same output as Q_3. [1]

.....

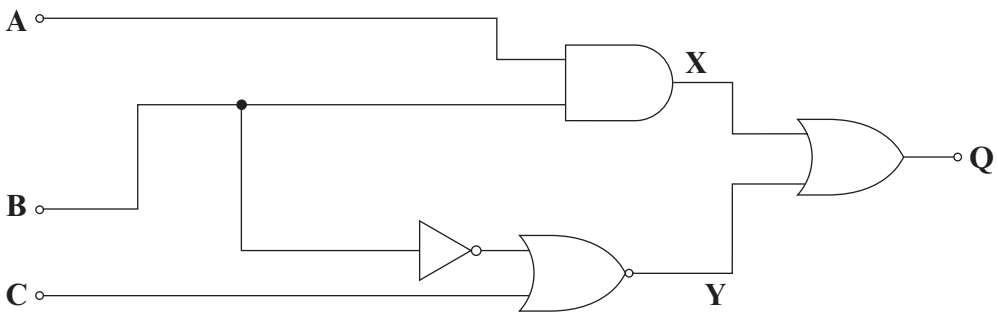
Examiner only

(d) Show how the output Q_3 could be generated using a multiplexer. [1]



Examiner only

2. A system of logic gates is shown below.



(a) Complete the truth table for this system. [3]

C	B	A	X	Y	Q
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

(b) (i) Redraw this logic system using NAND gates only. [3]

(ii) Draw lines through all redundant gates. Identify each redundant pair. [3]

Examiner only

3. *(a)* Simplify the following expression. [1]

$\overline{C}.C$ = ...

(b) Using a Karnaugh map or Boolean algebra simplify the following expression as much as possible. [4]

$Q = D.C.B + \overline{D}.\overline{C}.B.\overline{A} + D.\overline{C}.A + D.B.\overline{A}. + D.\overline{C}.\overline{B}.A$

.....

.....

.....

.....

.....

DC \ BA	00	01	11	10
00				
01				
11				
10				

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. [2]

$$Q = \overline{C.\overline{A}.C}$$

.....

.....

.....

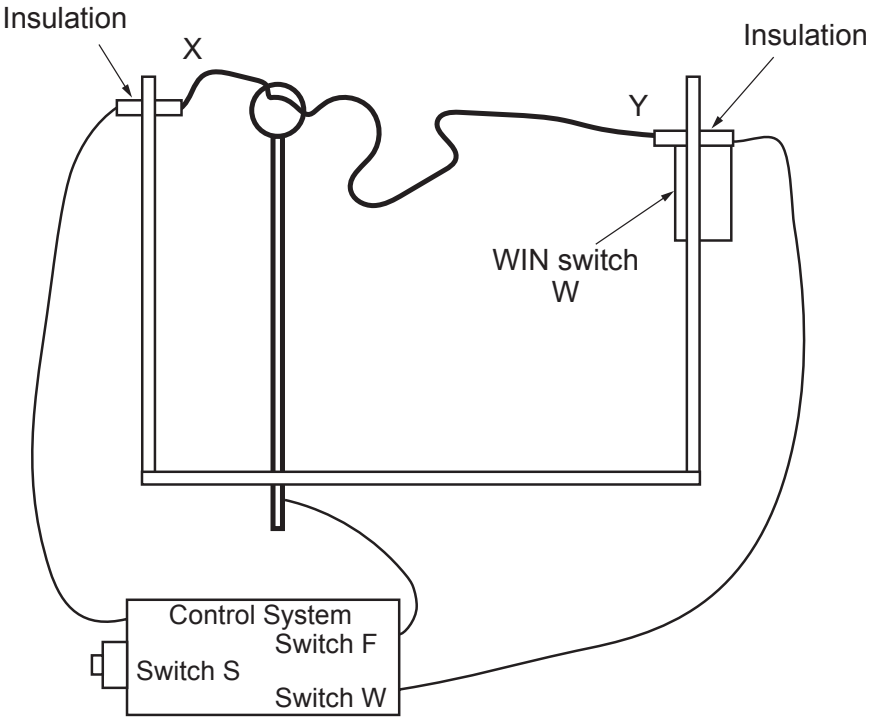
1141 010007

Turn over.

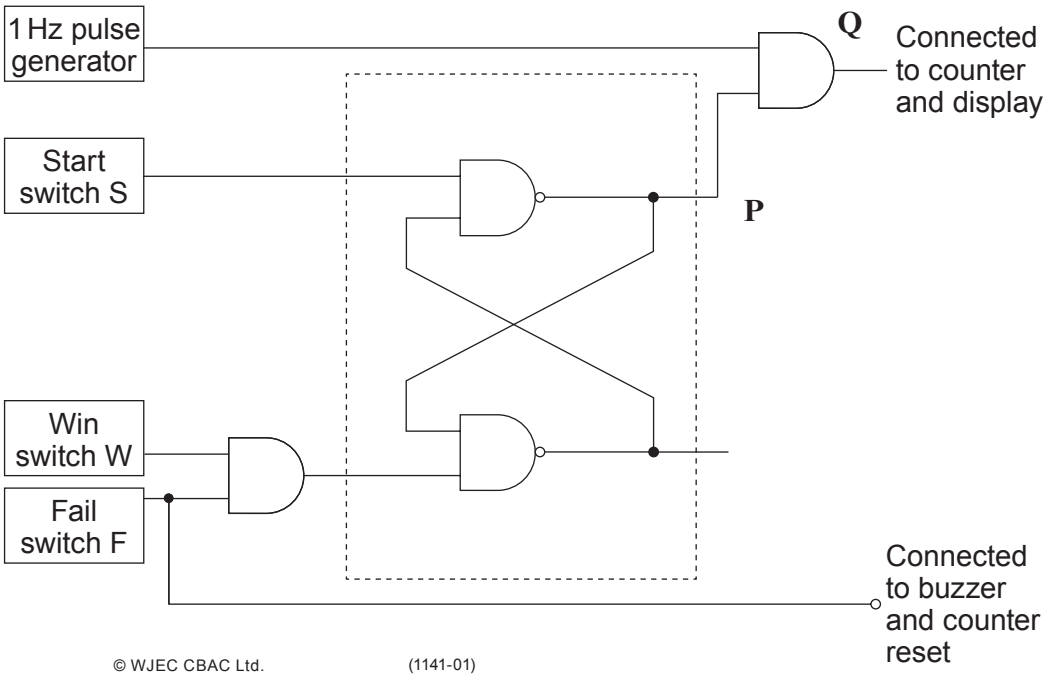
4. A student's design for a **'steady-hand'** game is shown below.

- When the START switch S is pressed the counter starts and the contestant moves the metal loop along the wire from point X to point Y as quickly as possible.
- If the metal loop reaches WIN switch W without touching the wire the count shown on the display indicates the time taken.
- If the loop touches the wire before the point Y this acts as a FAIL switch F and the counter resets and a buzzer sounds.

Switches S, W and F are active low.



Part of the control system is shown below.



Examiner only

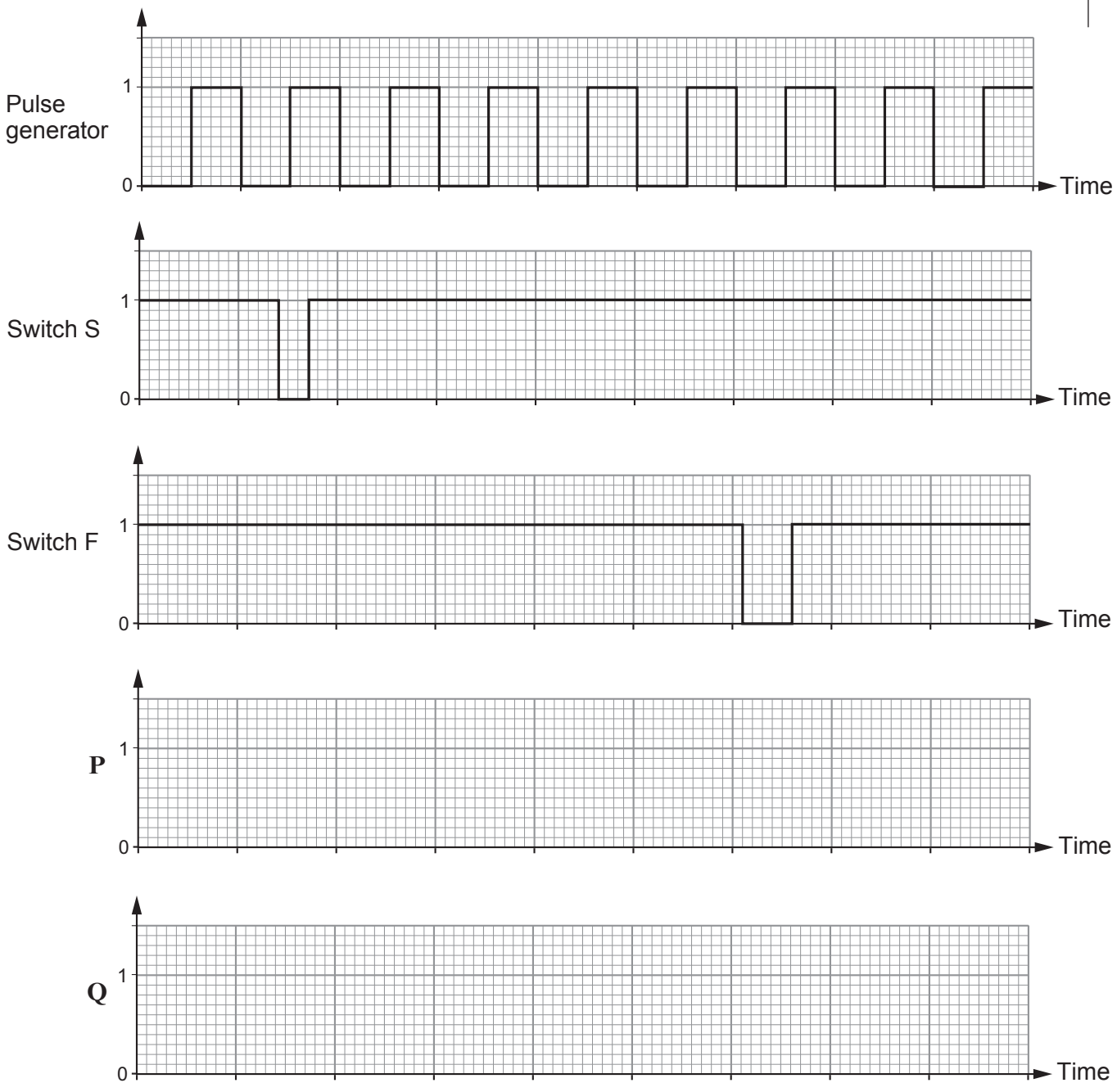
(a) What name is given to the sub-system shown in the dashed box? [1]

.....

(b) Whilst being attempted the loop touches the wire part way along. The timing diagram below shows:

- the output from the pulse generator
- the signal from switch S
- the signal from switch F

(i) Complete the diagram to show the outputs P and Q. [3]



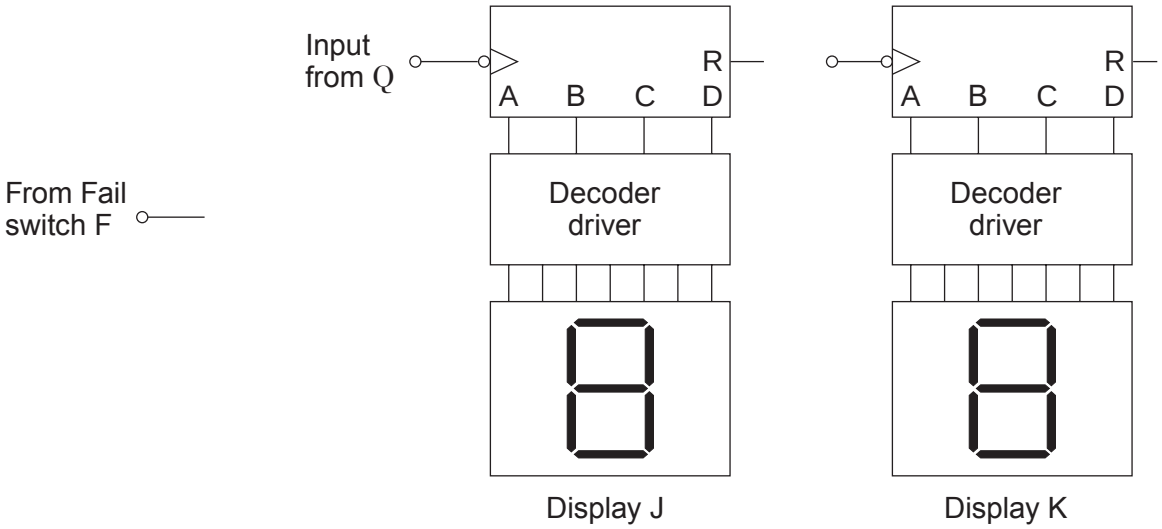
(ii) How many pulses will be fed into the counter/display? [1]

.....

1141 010009

Examiner only

(c) The counter/display sub-system is shown below.



Each counter resets automatically on the tenth pulse.

(i) What type of counter is this? [1]

.....

The counters are falling-edge-triggered.

(ii) **Complete the diagram** so that the display can show a maximum of '99'. [1]

(iii) A player takes 25 s to complete the game successfully. Which display, J or K shows the number 2? [1]

.....

(d) Switch F can reset both counters. Explain how this can be achieved.
(You can either write below or draw your solution on the diagram.) [2]

.....

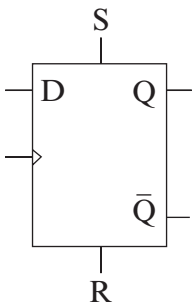
.....

.....

BLANK PAGE

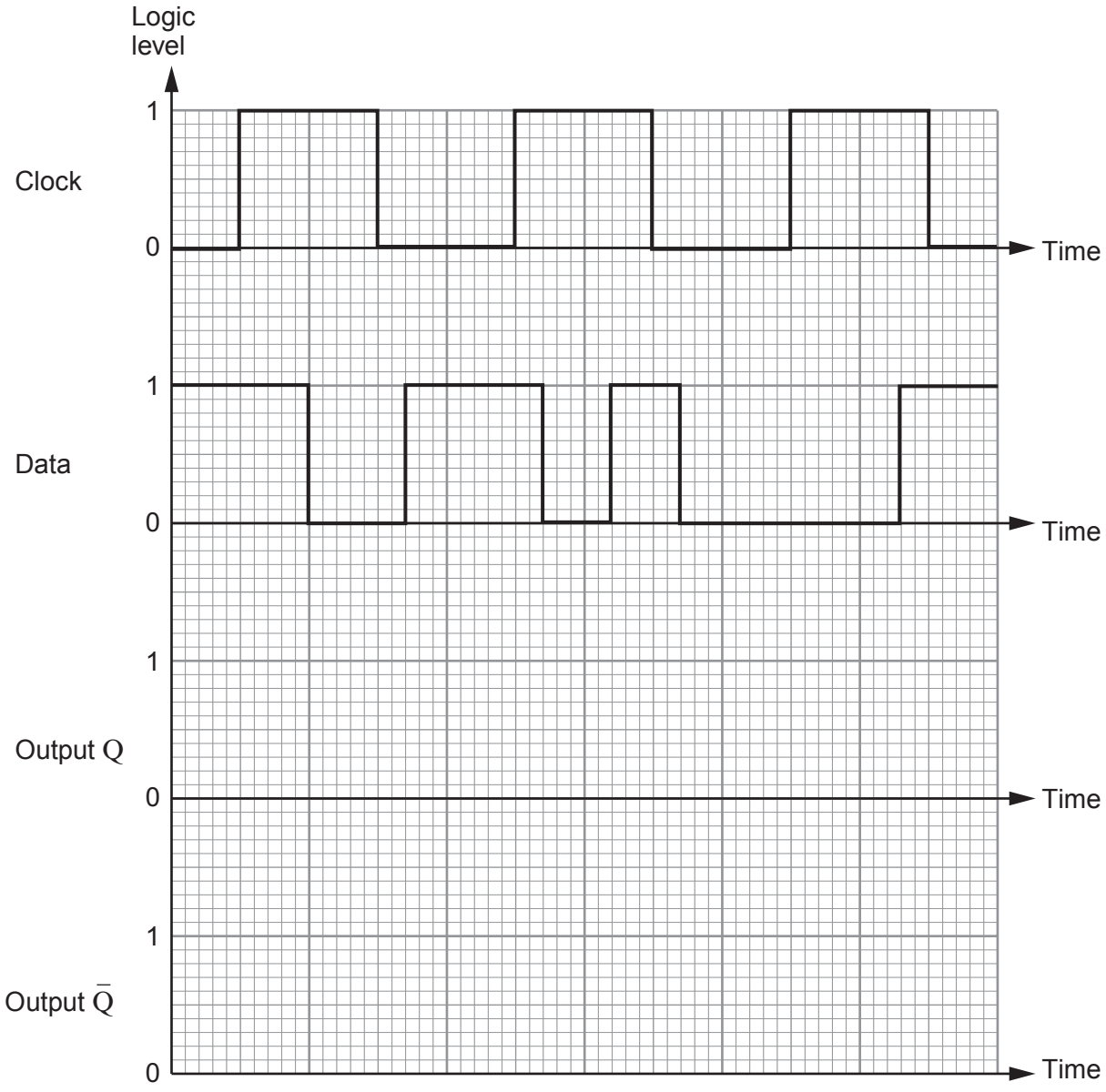
Examiner only

5. *(a)* The D-type flip-flop in the diagram is rising-edge triggered.



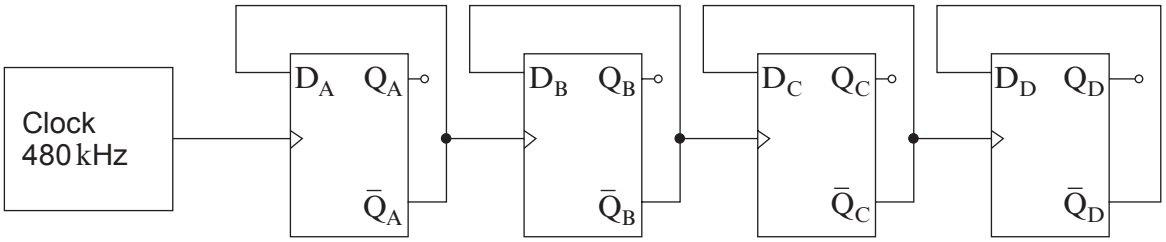
The signals applied to the clock and data inputs are shown below.

Complete the timing diagram for the Q and $\bar{Q}$ outputs. [2]



Examiner only

(b) The clock in the following diagram produces a square wave output of 480 kHz. This is fed into the series of 4 D-type flip-flops shown below. The D-type flip-flops are rising-edge triggered.



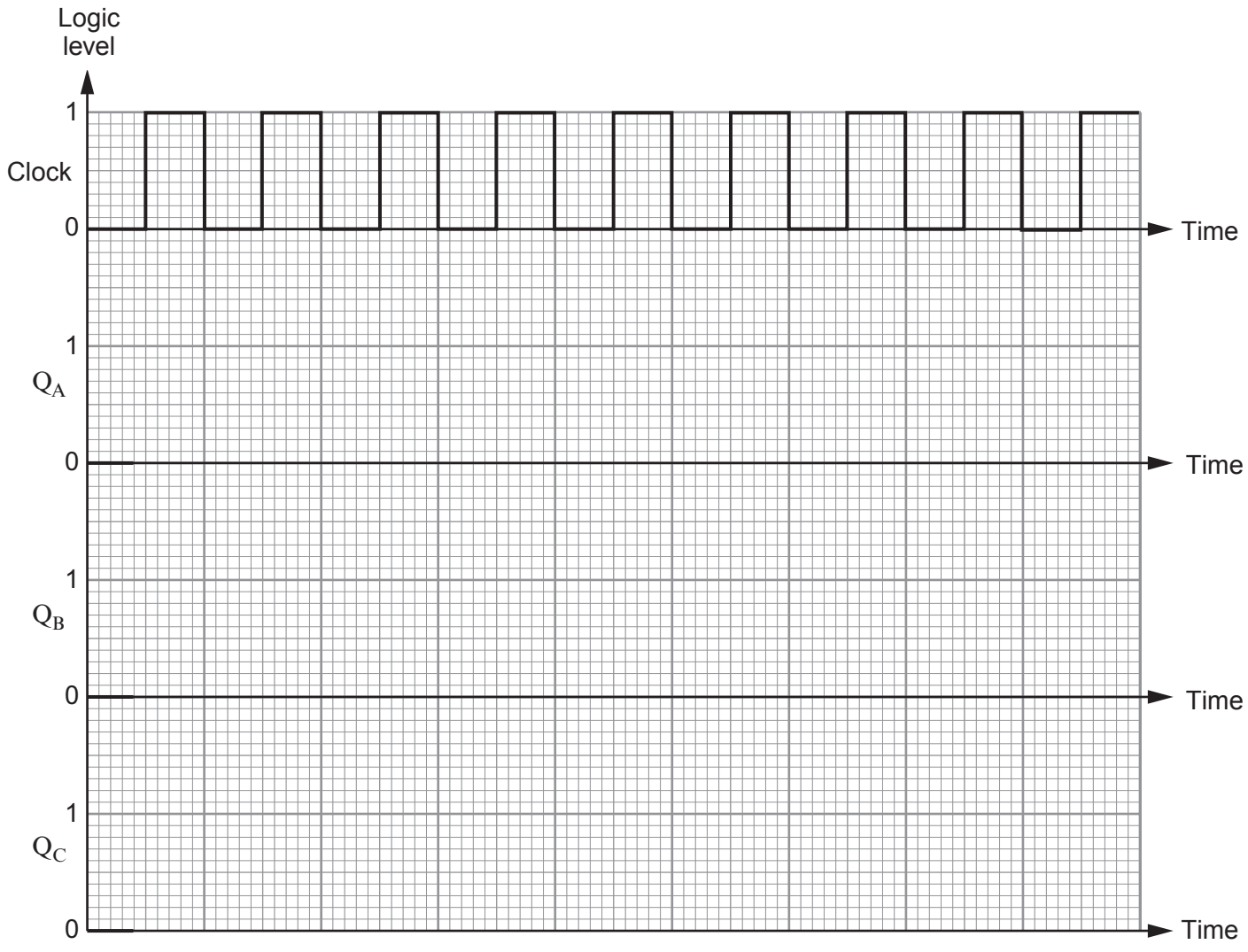
(i) What is the frequency at the output Q_A? [1]

.....

(ii) Which output will produce a frequency of 60 kHz? [1]

.....

(iii) The timing diagram below shows the output from the clock. Complete the diagram to show the signal at outputs Q_A, Q_B and Q_C. [3]



Turn over.

Examiner only

6. *(a)* Ideal operational amplifiers have some characteristics that should be either infinite or zero. Complete the table below by putting either **infinite** or **zero** to indicate the desired value. [2]

Characteristic	Infinite or zero
Open loop gain	
Input impedance	
Output impedance	
Slew-rate	

(b) Practical voltage amplifiers should have a very high gain-bandwidth product.

(i) Define bandwidth for a voltage amplifier. [1]

.....

.....

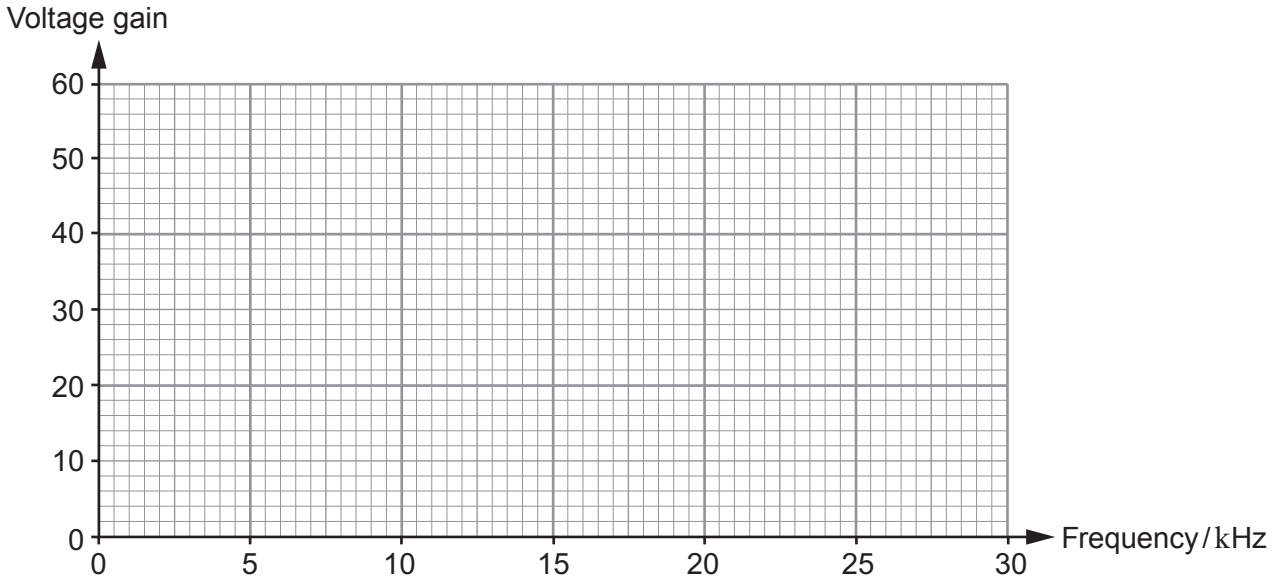
(ii) A voltage amplifier with a gain-bandwidth product of 3 MHz is configured to have a voltage gain of 500. Calculate the bandwidth. [1]

.....

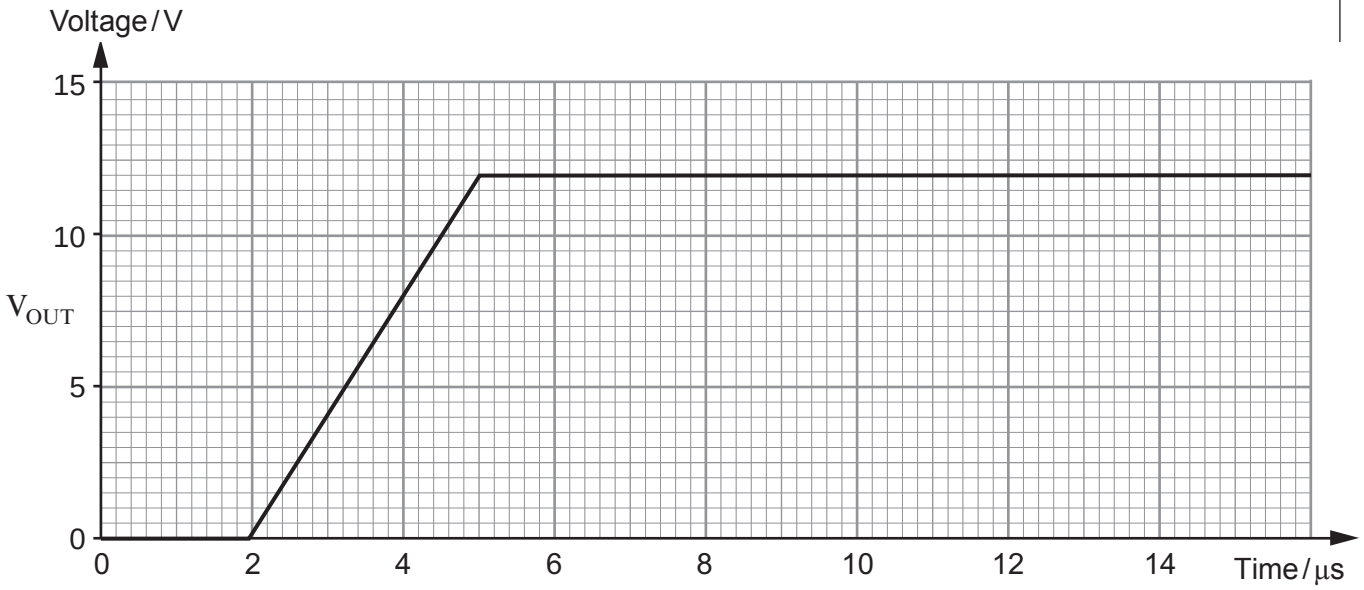
.....

Examiner only

(c) (i) Another amplifier has a voltage gain of 50 with a bandwidth of 22 kHz. Sketch the frequency response of this amplifier on the axes below. [2]



(ii) The graph shows how the output voltage of the amplifier responds to a **large** step input voltage.



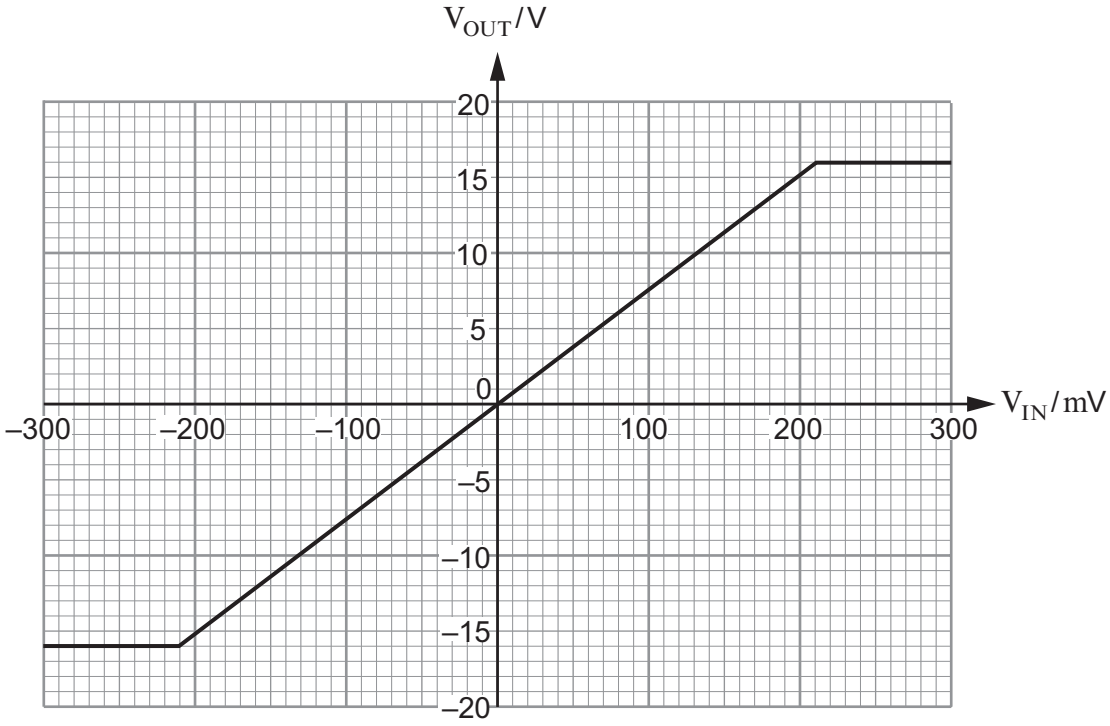
Calculate the slew rate of this amplifier and give an appropriate unit. [2]

.....

.....

Examiner only

7. The graph shows the characteristic of a non-inverting op-amp voltage amplifier.



(a) Use the graph to determine:

(i) the saturation voltage; [1]

.....

.....

(ii) the voltage gain of this amplifier. [1]

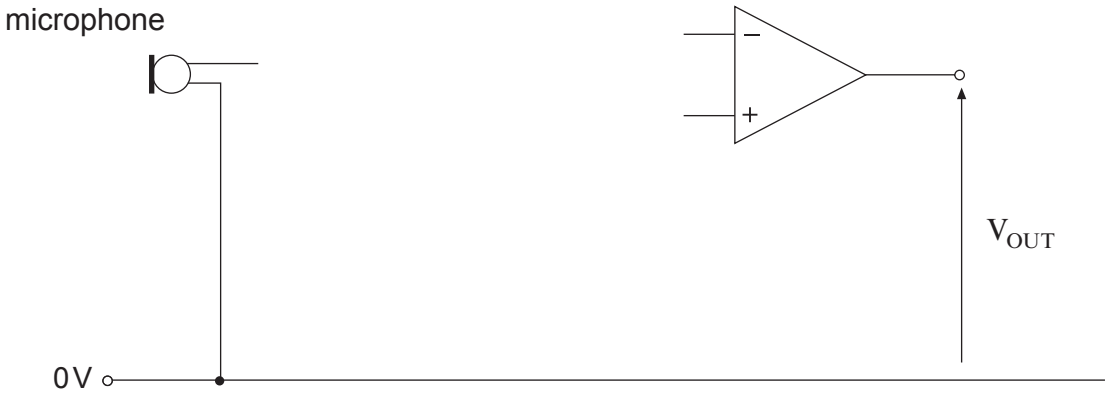
.....

.....

Examiner only

The amplifier is modified to have a voltage gain of 80 and it is used to amplify the signal from a microphone.

(b) (i) Complete the circuit diagram for this amplifier. [3]



(ii) Choose suitable resistor values to give the amplifier the voltage gain of 80. Label the circuit diagram with these values. [2]

.....

.....

.....

(c) Calculate the maximum output voltage of the microphone that avoids clipping distortion. [1]

.....

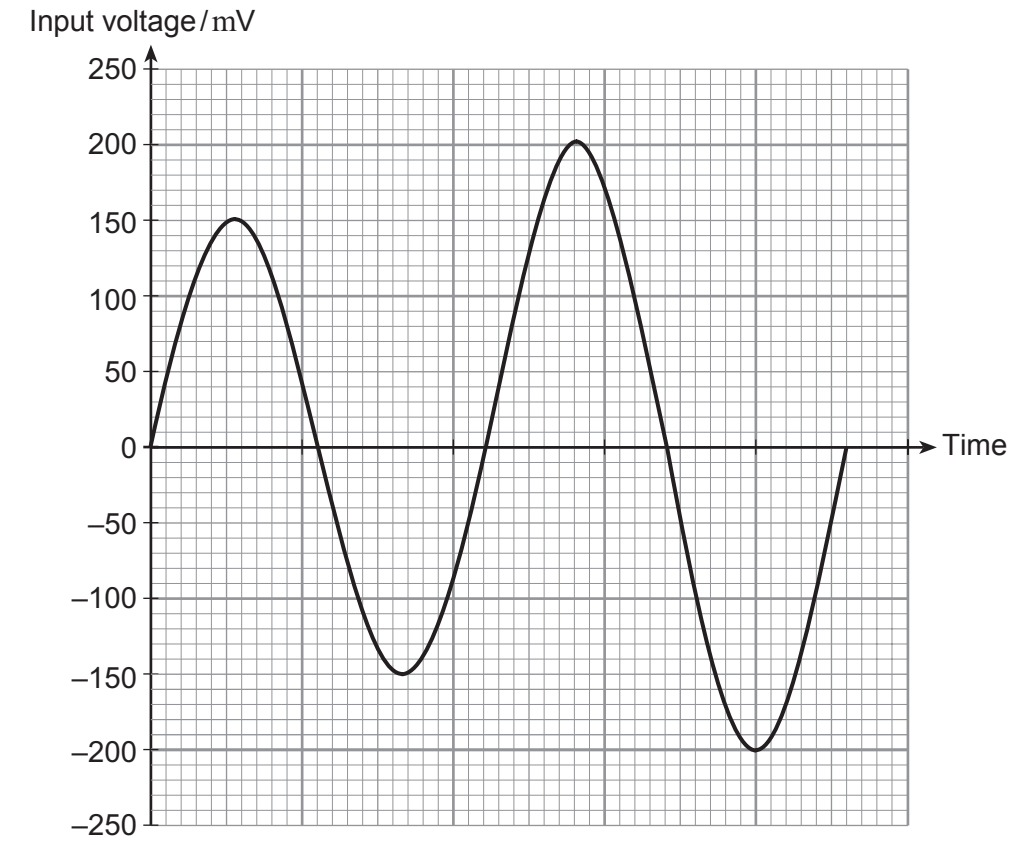
.....

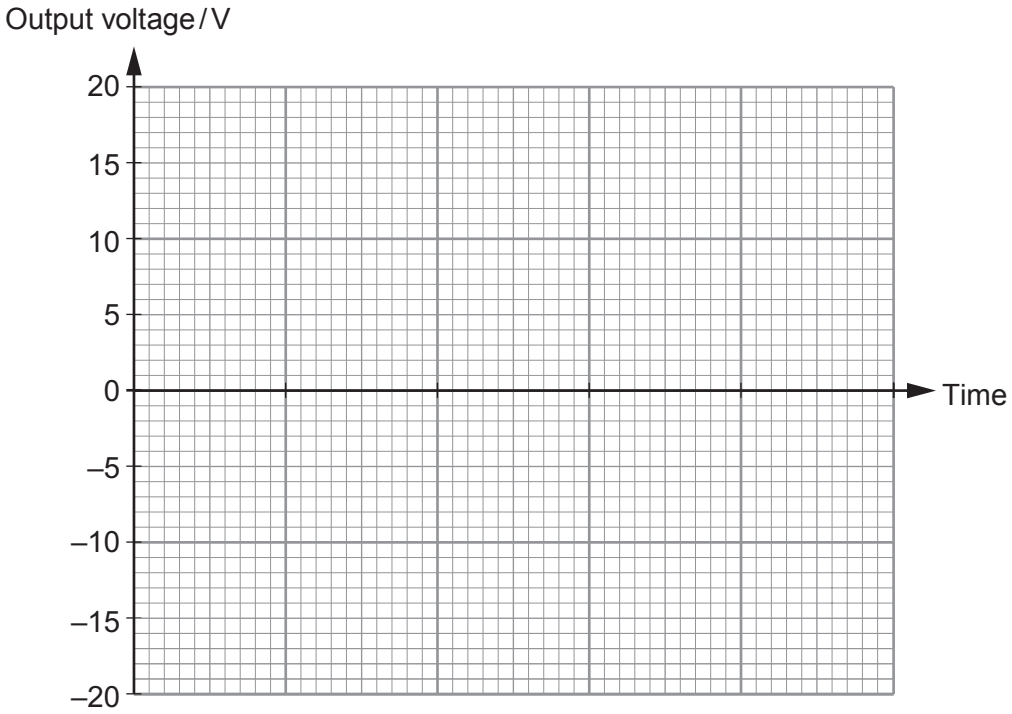
TURN OVER FOR THE LAST PART OF THE QUESTION.

Examiner only

The output signal of the microphone is shown below.

(d) Sketch the output produced by the amplifier. [3]





END OF PAPER

BLANK PAGE