Surname	Centre Number	Candidate Number
Other Names		2

GCE A Level

1145/01

S17-1145-01

ELECTRONICS – ET5

WEDNESDAY, 14 JUNE 2017 – AFTERNOON

1 hour 30 minutes

For Examiner's use only		
Question	Maximum Mark	Mark Awarded
1.	7	
2.	10	
3.	5	
4.	10	
5.	6	
6.	9	
7.	6	
8.	10	
9.	7	
Total	70	

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ADDITIONAL MATERIALS

A calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.
Write your name, centre number and candidate number in the spaces at the top of this page.
Answer **all** questions.
Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 70.
The number of marks is given in brackets at the end of each question or part-question.
You are reminded of the necessity for good English and orderly presentation in your answers.
You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Alternating Voltages $V_o = V_{rms}\sqrt{2}$

Silicon Diode $V_F \approx 0.7\,V$

Operational amplifier

$G = -\dfrac{R_F}{R_{IN}}$ Inverting amplifier

$G = 1 + \dfrac{R_F}{R_1}$ Non-inverting amplifier

$V_{OUT} = V_{DIFF}\left(\dfrac{R_F}{R_1}\right)$ Difference amplifier

$V_{OUT} = -R_F\left(\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3}\right)$ Summing amplifier

$V_L \approx V_Z\left(1 + \dfrac{R_F}{R_1}\right)$ Stabilised power supply

Emitter follower $V_{OUT} = V_{IN} - 0.7\,V$

Filters

$f_b = \dfrac{1}{2\pi RC}$ Break frequency for high pass and low pass filters

$X_C = \dfrac{1}{2\pi fC}$ Capacitive reactance

Thyristor phase control

$\phi = \tan^{-1}\dfrac{R}{X_C}$

$\tan\phi = \dfrac{R}{X_C}$

Signal conversion $\text{resolution} = \dfrac{\text{i/p voltage range}}{2^n}$ ADC

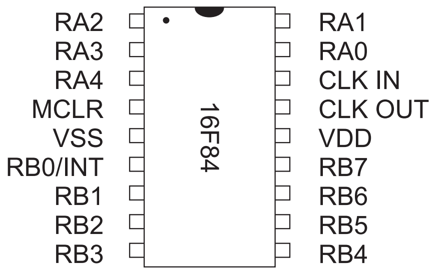
Power amplifier $P_{MAX} = \dfrac{V_S^2}{8R_L}$ where V_S is the rail-to-rail voltage

PIC Information

The PIC programs include ‘equate’ statements that define the following labels:

Label	Description
PORTA	input / output port A
PORTB	input / output port B
TRISA	the control register for port A
TRISB	the control register for port B
STATUS	the status register
INTCON	the interrupt control register
W	the working register (= h ‘0’)
F	the file register (= h ‘1’)
RP0	the register page selection bit 0
Z	the zero flag status bit
GIE	the global interrupt controller bit
INTE	the external interrupt enable bit

Pinout for 16F84 PIC IC:



List of commands:

Mnemonic	Operands	Description
bcf	f, b	Clear bit b of file f
bsf	f, b	Set bit b of file f
btfss	f, b	Test bit b of file f, skip next instruction if bit is set
call	k	Call subroutine k
clrf	f	Clear file f
goto	k	Branch to label k
movf	f, d	Move file f (to itself if d = 1, or to working register if d = 0)
movlw	k	Move literal k to working register
movwf	f	Move working register to file f
retfie		Return from interrupt service routine and set global interrupt enable bit GIE

Comparison of TASM and MPASM languages:

Version		**TASM**	**MPASM**
Number system notation	Decimal	153	d'153'
	Hex	$2B	h'2B' or 0x2B
	Binary	%10010110	b'10010110'
Opcode Notation		.equ	equ
		.org	org
		.end	end
		label:	label

Structure of the INTCON register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF

Structure of the STATUS register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRP	RP1	RP0	TO	PD	Z	DC	C

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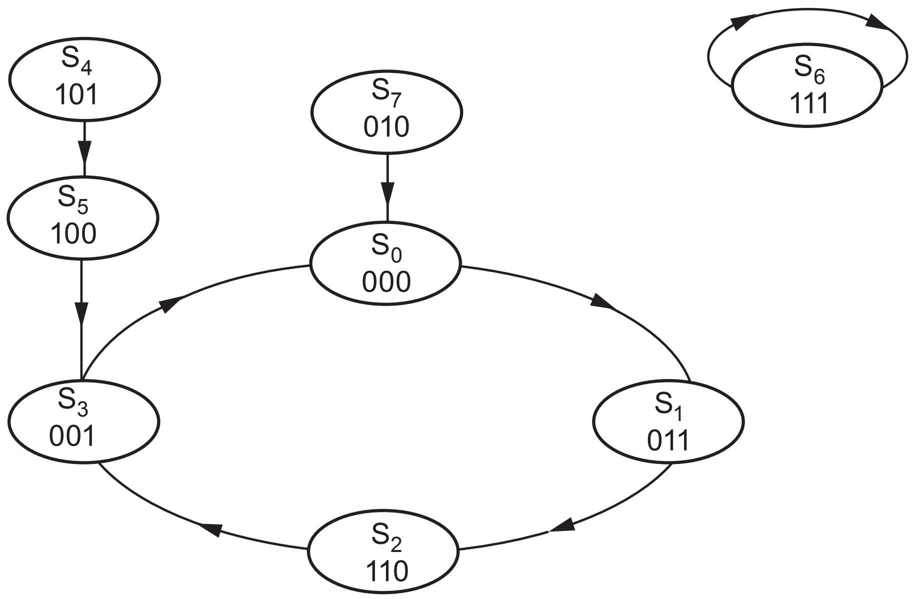
Answer **all** *questions.*

1. *(a)* Here is the state diagram for a sequence generator.



(i) Identify any stuck state(s). [1]

....

(ii) Identify **one** unused state which is not stuck. [1]

....

(iii) On power-up, the system starts in state S_4.
How many clock pulses are needed to reach state S_1? [1]

....

Examiner only

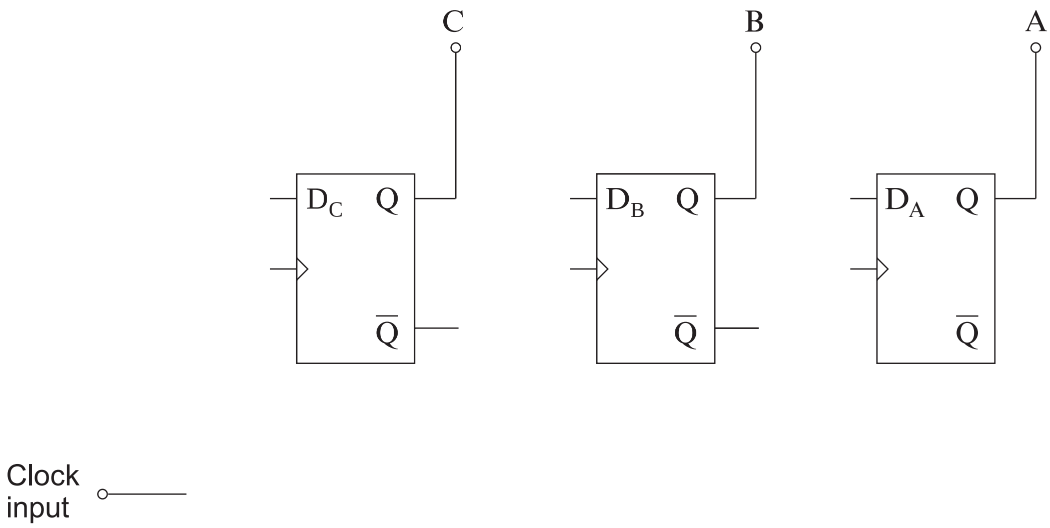
(b) A **different** sequence generator is governed by the following Boolean equations:

$D_A = C$

$D_B = \overline{A + C}$

$D_C = \overline{B \cdot C}$

Complete the circuit diagram for this sequence generator. [4]



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2. A student designs a simple tone generator based on a synchronous counter and a DAC. The synchronous counter produces a digital ramp output which the DAC converts into a triangular wave.

(a) The 3-bit synchronous counter is built using three D-type bistables, logic gates and a clock.

It:
- counts up, in stages, from ‘000’ to ‘111’;
- then counts down in stages to ‘000’;
- and does so repeatedly.

The table shows the sequence.

State	Current Outputs			Next Outputs		
	C	**B**	**A**	D_C	D_B	D_A
0	0	0	0			
1	0	1	0			
2	1	0	0			
3	1	1	0			
4	1	1	1			
5	1	0	1			
6	0	1	1			
7	0	0	1	0	0	0

(i) Complete the table. [1]

(ii) The inputs to the D-types are controlled by Boolean expressions linking D_C, D_B and D_A to the counter outputs **C**, **B** and **A**.
Complete the expression for D_A **(only)**. [2]
(Extra credit will be given for using the simplest Boolean expression.)

....

....

....

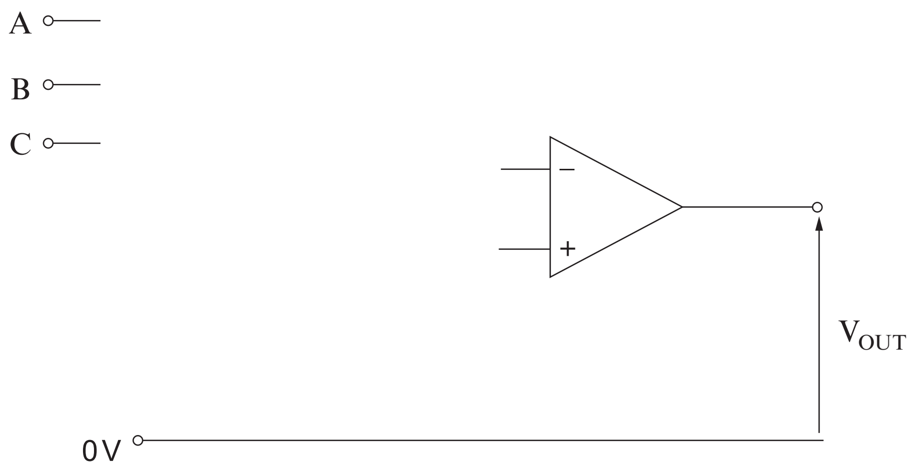
....

D_A = ...

Examiner only

(b) The signals **C**, **B** and **A** (lsb) are applied to the inputs of a 3-bit DAC.
It is built from an op-amp and four resistors – 200 kΩ, 100 kΩ, 50 kΩ and 10 kΩ.

(i) Complete the circuit diagram for this DAC. [2]



(ii) Label all resistors with their resistance values. [2]

(iii) Logic 1 signals are represented by 12 V and logic 0 by 0 V.
Calculate the value of V_{OUT} when the input signals are C = 1, B = 0, A = 1. [1]

....

....

(c) (i) How would the student increase the frequency of the tone produced by the tone generator? [1]

....

....

(ii) How would the student increase the amplitude of the tone produced by the tone generator? [1]

....

....

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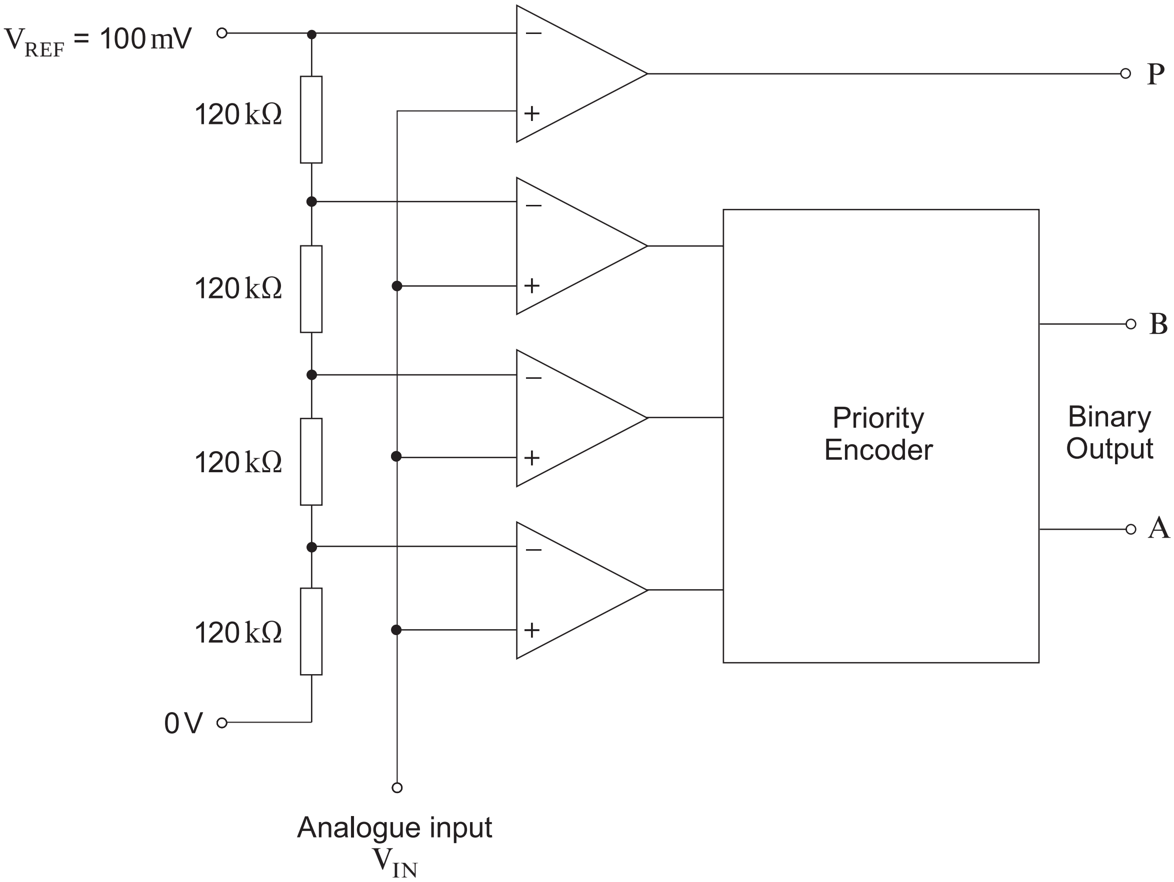
3. The binary output for the two-bit flash ADC shown below increases uniformly as V_{IN} increases.



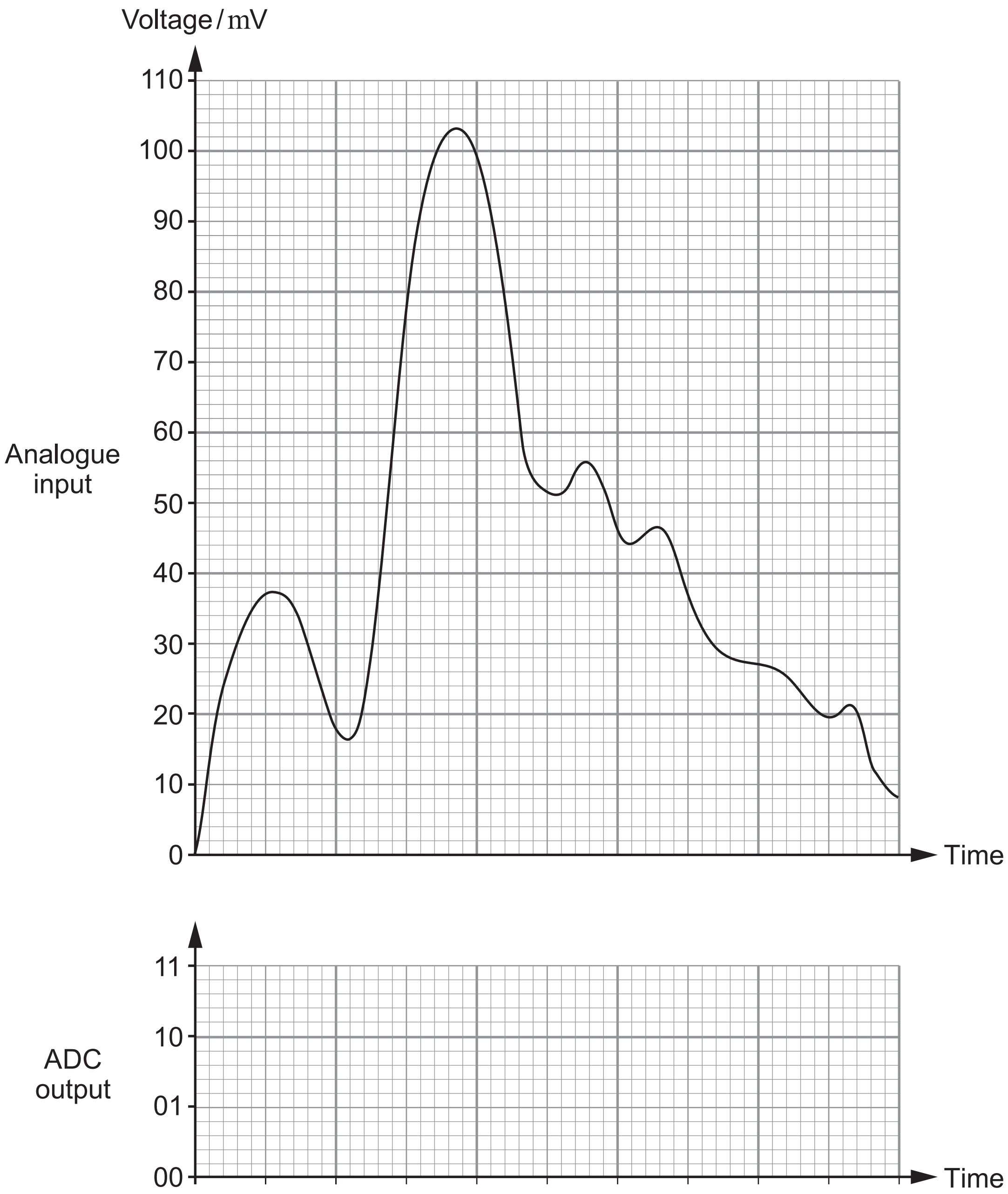
(a) Calculate the resolution of this ADC. [1]

....

....

Examiner only

(b) The analogue input signal is shown in the upper graph.
Use the axes provided to draw the resulting ADC output signal. [3]

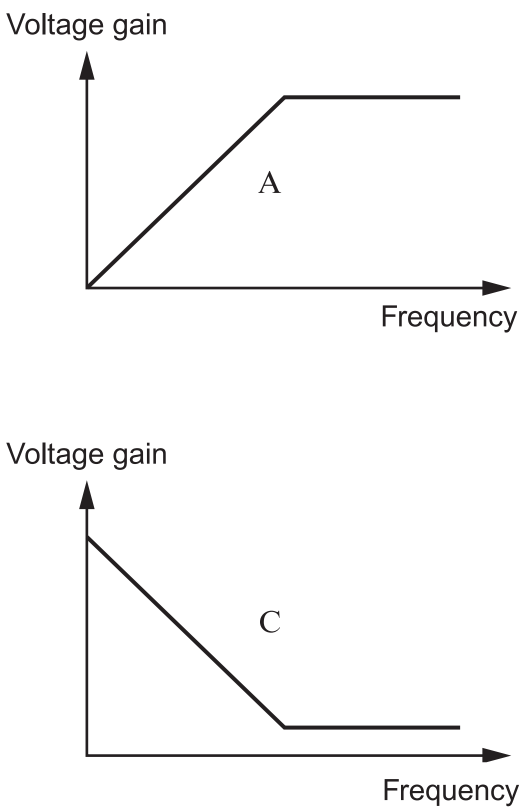


(c) On the analogue input graph above, add a cross and label it 'P' to show where the overflow output first becomes logic 1. [1]

Turn over.

Examiner only

4. *(a)* Here are the frequency response curves for four types of filter, plotted using log-log scales.



(i) Which one represents the behaviour of an active treble boost filter? [1]

....

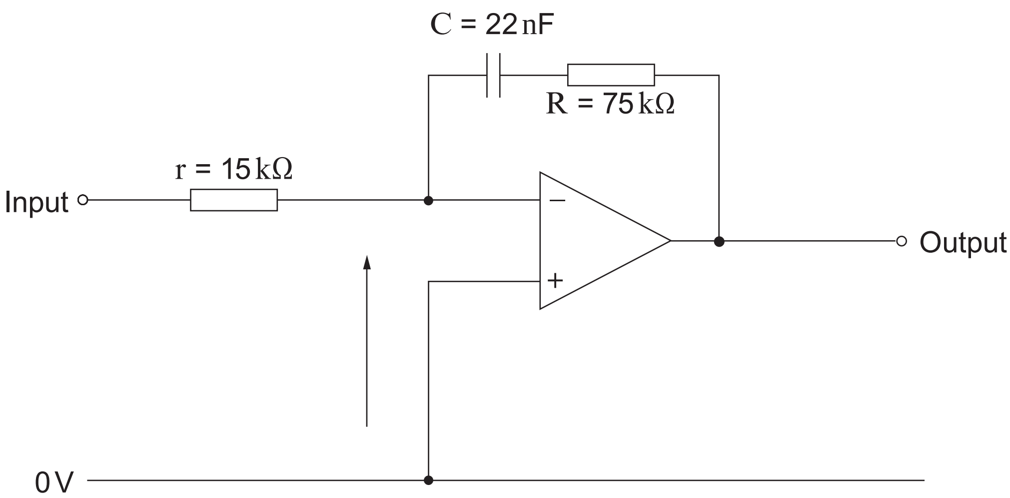
(ii) What problem might a treble boost filter encounter at a very high frequency? [1]

....

....

Examiner only

(b) An audio system includes the filter circuit shown below.



(i) Complete the equation that defines the term break frequency: [1]

At the break frequency, X_C = ...

(ii) Calculate the break frequency for the filter shown. [2]

....

....

....

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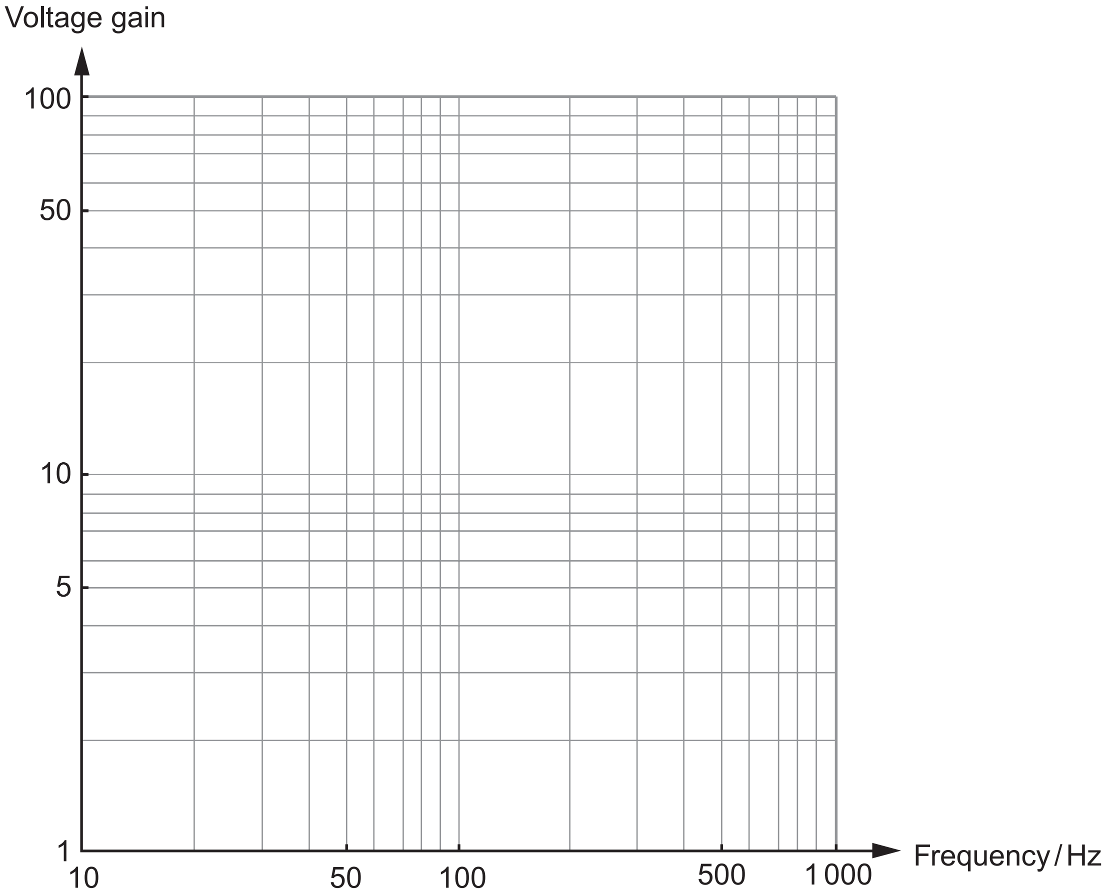
Examiner only

(iii) Use the axes provided to draw the frequency response for this filter. [3]



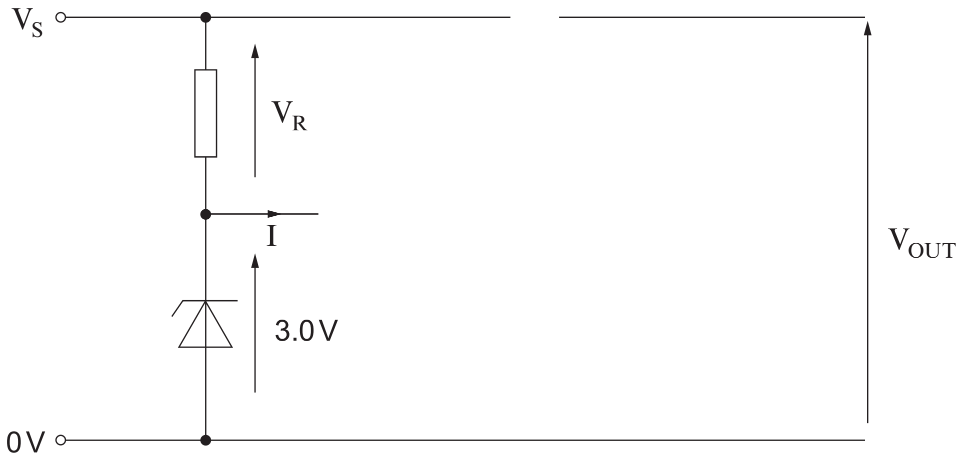
(iv) A sinusoidal signal of frequency 500 Hz and amplitude 100 mV is applied to the input of the filter. [2]

For the resulting output signal, what is:

- its frequency; ....
- its amplitude? ....

Examiner only

5. The diagram shows part of a voltage regulator, using a 3 V zener diode.



(a) The supply voltage V_S = 12 V. What is the voltage V_R across the resistor?

.... [1]

(b) The supply voltage V_S increases to 12.5 V. What is now:

the voltage V_Z across the zener diode; ....

the voltage V_R across the resistor? .... [1]

(c) (i) Complete the circuit diagram for the voltage regulator by adding:

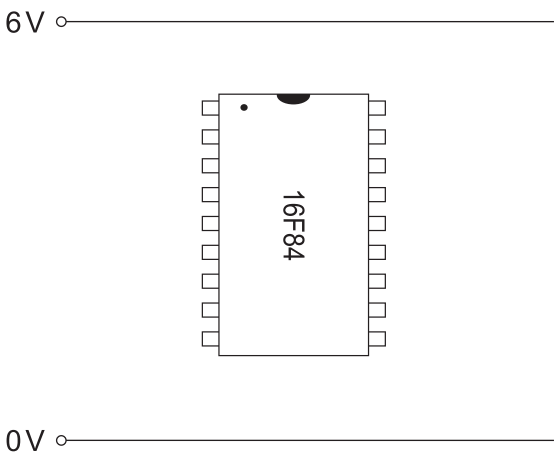
- a non-inverting amplifier, connected to monitor the reference voltage from the zener and the output voltage V_{OUT};
- an emitter follower, controlled by the non-inverting amplifier;
- a resistor network. [3]

(ii) Choose suitable resistor values to give an output voltage of 9.0 V. Label the resistors with these values. [1]

6. A home security system is controlled by a microcontroller system. Whenever the front door is opened, three LEDs, one red, one yellow and one blue, are lit in sequence to warn the occupants.

- A switch, concealed in the door frame, is **open** when the door is opened.
- It is connected to Port B, bit 0.
- Opening the door causes a microcontroller interrupt.
- The red LED connected to Port A bit 2.
- The yellow LED connected to Port A bit 1.
- The blue LED connected to Port A bit 0.

(a) Complete the diagram by showing how the switch and a $10\,\mathrm{k}\Omega$ resistor are connected to the microcontroller to cause an interrupt when the switch is **open**. [2]



(b) The Interrupt Service Routine (ISR) is given below. The ISR uses a three second delay subroutine called 'threesec'.

```
alarm   movwf   Wstore
        bsf     PORTA,2
        call    threesec
        bsf     PORTA,1
        call    threesec
        bsf     PORTA,0
        call    threesec
        call    threesec
        clrf    PORTA
        btfss   PORTB,0
        goto    repeat
        bcf     INTCON, 1
        ....... .......
        retfie
```

Examiner only

(i) In what order do the LEDs light when the Interrupt Service Routine is called? [1]

....

(ii) For how long does the blue LED light when the ISR runs once? [1]

....

(iii) For how long does the red LED light when the ISR runs once? [1]

....

(iv) What is the purpose of the instructions in lines 209 and 210 in the control system? [2]

....

....

....

(v) **Add the label 'repeat'** in the correct place in the program. [1]

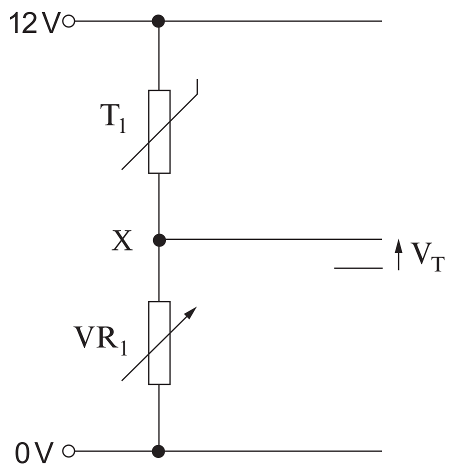
(vi) **Insert an instruction** in line 212 to recover the contents of the working register. [1]

Examiner only

7. Two thermistors, connected in a bridge circuit, are used to monitor the temperature of a fan-assisted oven. Thermistor T_1 is placed near the top of the oven and thermistor T_2 near the bottom.

The fan is switched on automatically when the temperature difference between top and bottom is too great.

The diagram shows part of the bridge circuit.



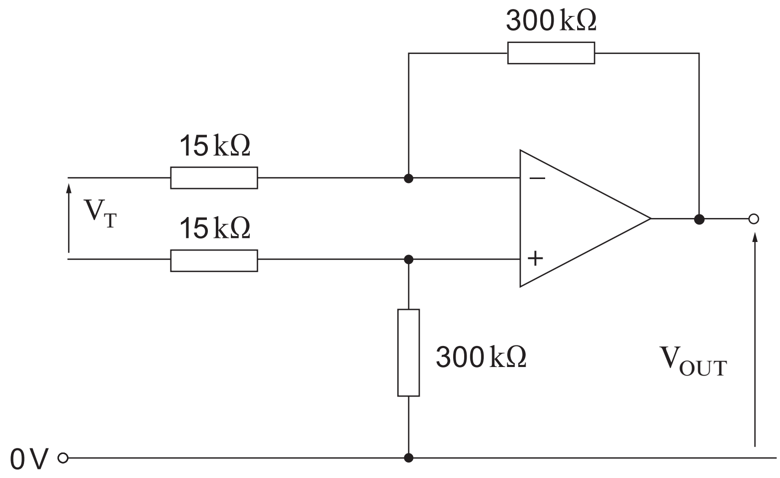
(a) (i) At room temperature, thermistor T_1 has a resistance of $1.1\,k\Omega$ and the variable resistor VR_1 is set to a resistance of $0.5\,k\Omega$.
Calculate the voltage at X at room temperature. [1]

....

(ii) **Complete the bridge circuit**. Voltage V_T must increase when the temperature difference between the top and bottom of the oven rises. [2]

Examiner only

(b) The output of the bridge circuit is amplified by the following difference amplifier.



Calculate the output voltage, V_{OUT} , when V_T = + 1.5 mV. [2]

....

....

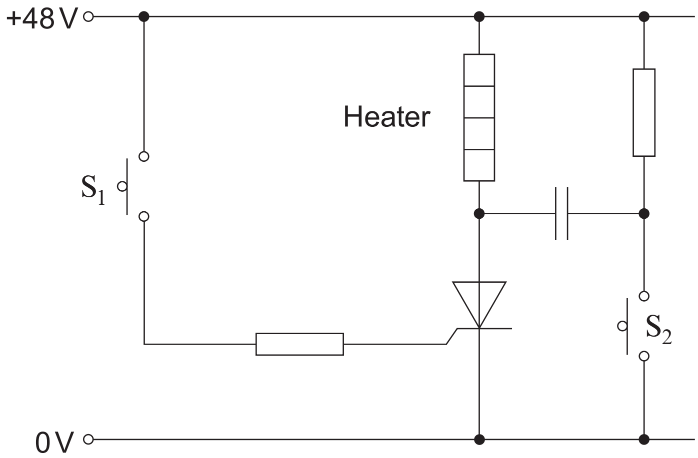
(c) What adjustment would make the fan switch on when the temperature difference is smaller? [1]

....

....

Examiner only

8. *(a)* The following diagram shows a thyristor used to control an electrical heater in a DC switching circuit.



(i) State the **purpose** of:

- switch S_1
- switch S_2

in this circuit. [2]

S_1 ....

S_2 ....

(ii) The table gives some data for the thyristor used in this circuit.

Property	**Typical value**
Max. forward current	25 A
Holding current	20 mA
Minimum gate current	10 mA
Gate voltage	1.5 V
Peak reverse voltage	800 V

What is the minimum current through the heater needed to keep the thyristor latched on? [1]

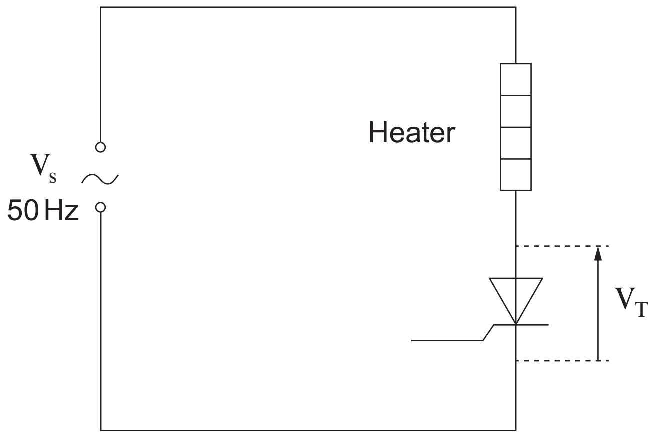
....

Examiner only

(b) In an AC circuit, a heater can be controlled using phase control.

(i) Add the variable resistor and capacitor needed for this control. [1]

(ii) Add a diac connected to reduce the turn-on time of the thyristor. [1]



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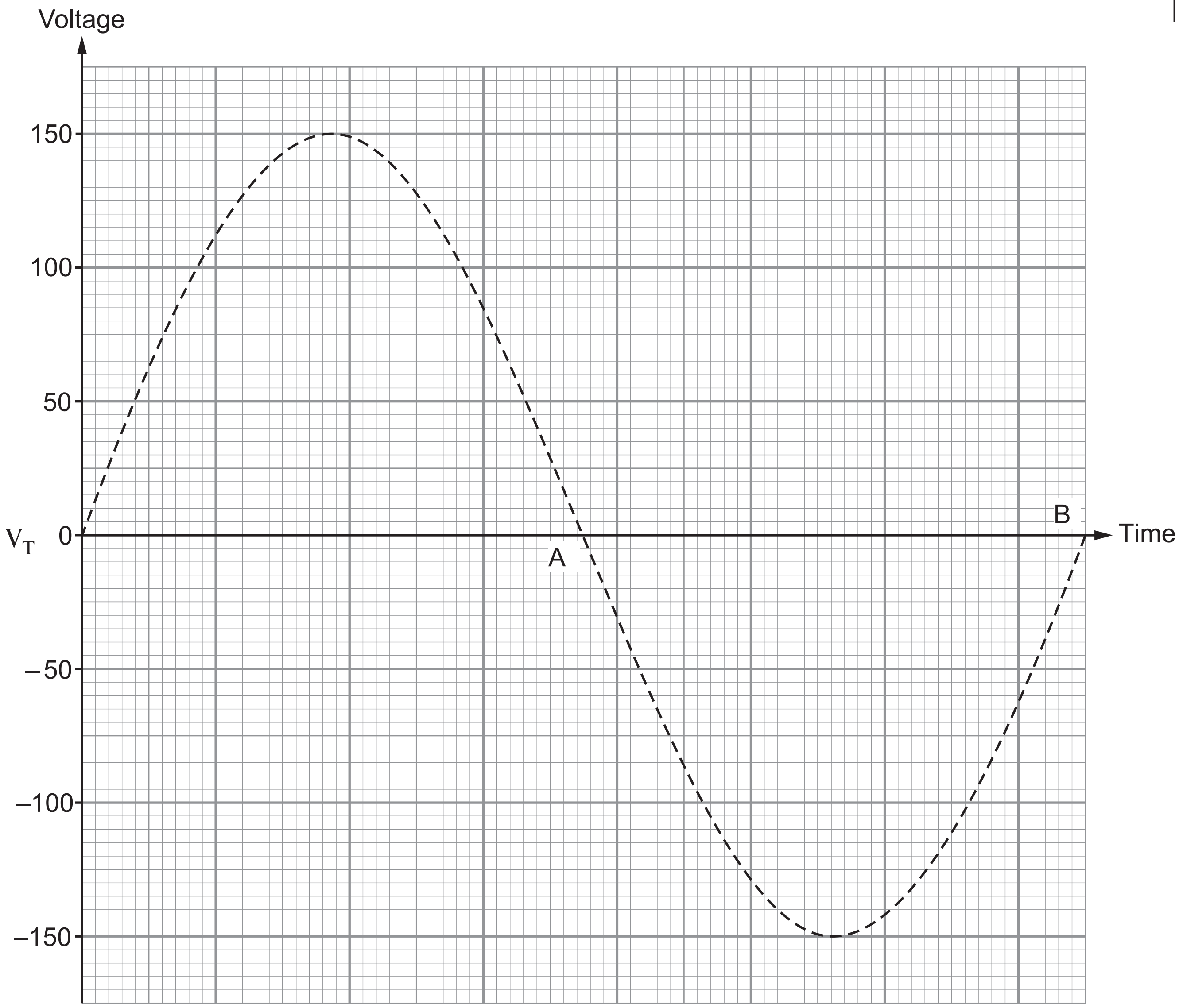
(iii) The diac switches on at 40 V. Use the axes provided to draw the voltage V_T across the thyristor. [3]
(The dotted trace shows one cycle of the applied AC supply voltage.)



(iv) What is the voltage across the heater between points A and B of the AC supply voltage? [1]

....

(v) The circuit uses a 1 μF capacitor. When the phase shift is 43°, what is the resistance of the variable resistor? [1]

....

....

....

....

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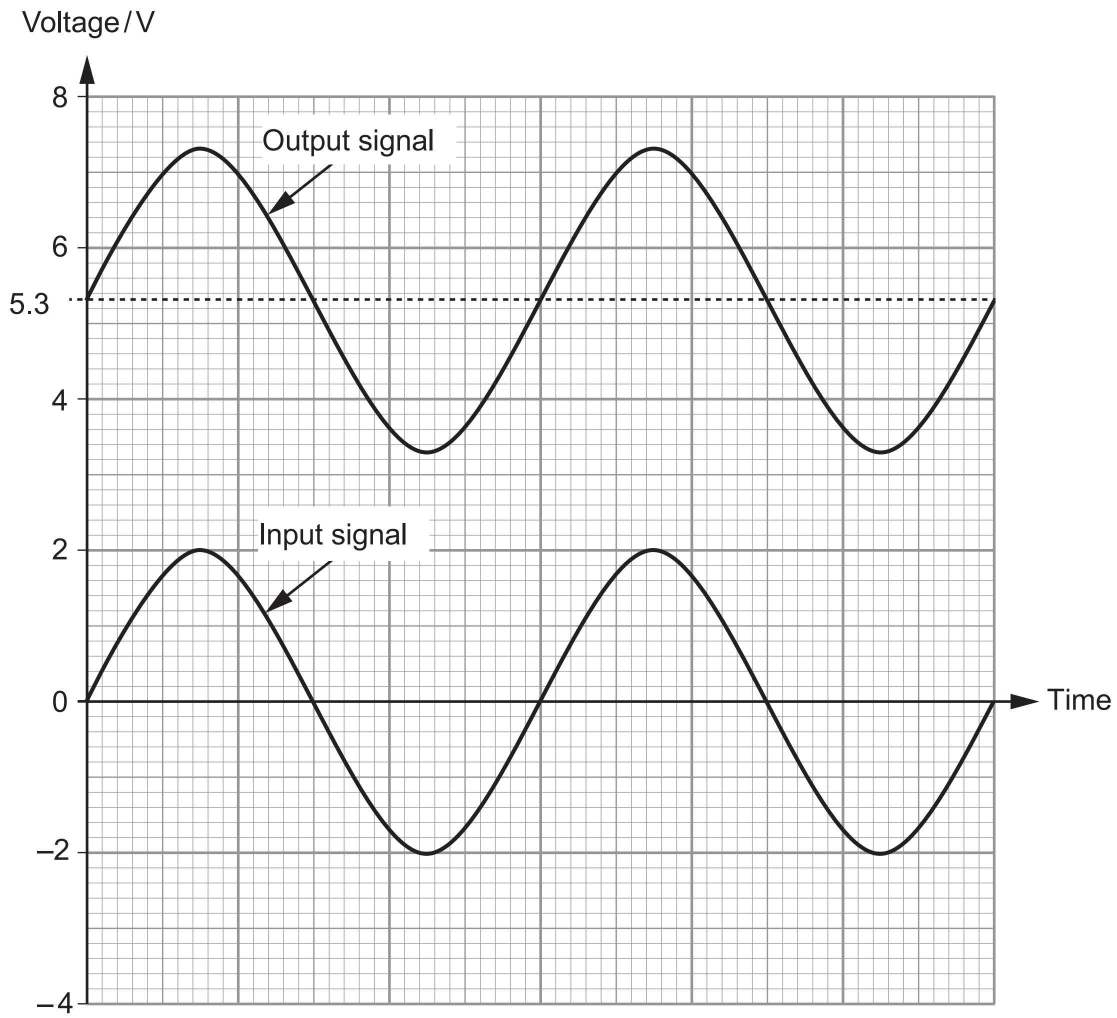
TURN OVER FOR THE LAST QUESTION.

9. An audio system uses an emitter follower sub-system, with resistor bias, as its power amplifier stage. The output and input signals for the emitter follower sub-system are shown below.



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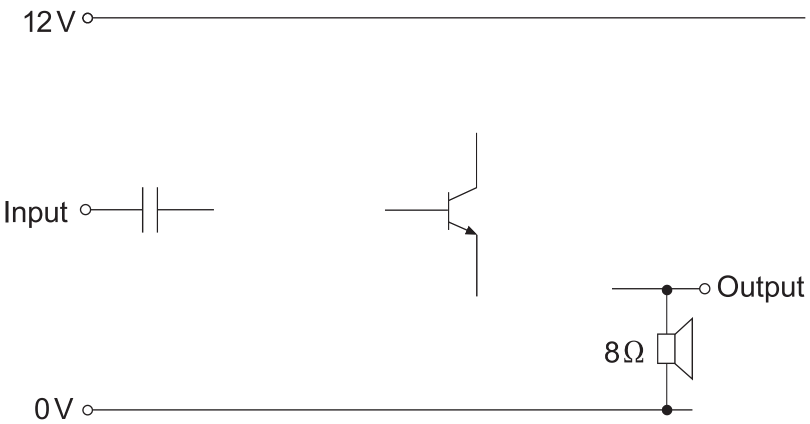
(a) Complete the circuit diagram so that it produces the output signal shown for the given input signal.

- Add any resistors needed, labelled with suitable values.
- Add all connections needed. [3]



(b) Comparing the emitter follower with the push-pull power amplifier, give:

(i) **one** advantage of using the emitter follower power amplifier. [1]

....

....

(ii) **one** disadvantage of using the emitter follower power amplifier. [1]

....

....

(c) Calculate the power dissipated **in the transistor** when there is no AC signal present. [2]

....

....

END OF PAPER

