GCE MARKING SCHEME

SUMMER 2017

ELECTRONICS - ET1
1141/01

INTRODUCTION

This marking scheme was used by WJEC for the 2017 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

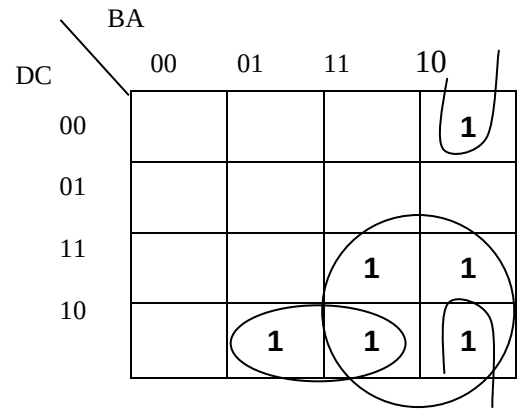
WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

GCE ELECTRONICS - ET1

SUMMER 2017 MARK SCHEME

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>1.</td><td>(a)</td><td>(i)
(ii)</td><td>NAND gate
<table><tr><td>B</td><td>A</td><td>Q_1</td><td>Q_2</td><td>Q3</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr></table>Q_2 and Q_3 correct one mark each</td><td>1

2</td></tr>
<tr><td></td><td>(b)</td><td></td><td>$Q_1 = \overline{A.B}$ or $\overline{A} + \overline{B}$
$Q_2 = A \oplus B$ or $A.\overline{B} + \overline{A}.B$
$Q_3 = A.B$</td><td>1
1
1</td></tr>
<tr><td></td><td>(c)</td><td></td><td>AND gate</td><td>1</td></tr>
<tr><td></td><td>(d)</td><td></td><td>D_3 to 5 V, others inputs to 0 V</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>8</td></tr>
<tr><td>2.</td><td>(a)</td><td></td><td><table><tr><td>C</td><td>B</td><td>A</td><td>X</td><td>Y</td><td>Q</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr></table></td><td></td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>One mark each correct column X, Y and Q</td><td>3</td></tr>
<tr><td></td><td></td><td></td><td>Correct replacement of AND with NAND
Correct replacement of both NOT and NOR with NAND
Correct replacement of OR with NAND</td><td>1
1
1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>3 correctly identified redundant pairs (one mark each)</td><td>3</td></tr>
<tr><td></td><td></td><td></td><td></td><td>9</td></tr>
</table>

Question			Marking detail	Marks available
3.	(a)		$\overline{C}.C = 0$	1
	(b)			
			Correct map One group of 4 and two of 2 identified (ecf map) Any correct term from groups identified Simplest overall expression	1 1 1 1
	(c)		Q = D.B + $\overline{C}.B.\overline{A}$ + D.$\overline{C}$.A	
			Q = $\overline{C}$ + (A.C) or $\overline{C}$ + ($\overline{\overline{A.C}}$) 1 mark (DeMorgan) $\overline{C}$ + A 1 mark (simplification)	1 1
				7
4.	(a)		Bistable (latch) or $\overline{S}\,\overline{R}$ Flip Flop or $\overline{S}\,\overline{R}$ Latch	1
	(b)	(i)	P switches between falling edge of switch S and falling edge of switch F P logic 1 between these points Q shows 5 pulses within envelope of P	1 1 1
		(ii)	5 (pulses)	1
	(c)	(i)	BCD counter	1
		(ii)	Output D of 1st counter to Clock of 2nd counter	1
		(iii)	[display] K	1
	(d)		(Switch) F connected to reset of **both** counters Via a NOT gate	1 1
				10

Question			Marking detail	Marks available
5.	(a)		Q logic1 between 1st and 3rd rising-edge of the clock $\overline{Q}$ inverse of Q	1 1
	(b)	(i)	240 kHz	1
		(ii)	Q_C or $\overline{Q}_C$	1
		(iii)	(All diagrams have mark/space ratio of 1:1) Q_A Pulse length 2×clock with rising edge on 'odd' clock pulse rising-edges. Q_B duration 4 ×clock and Q_C duration 8 × clock (both answers needed) Q_B First rising-edge on first falling-edge of A } Q_C First rising-edge on first falling-edge of B } (both answers needed)	1 1 1
				7
6.	(a)		<table><tr><th>Characteristic</th><th>Infinite or zero</th></tr><tr><td>Open loop gain</td><td>infinite</td></tr><tr><td>Input impedance</td><td>infinite</td></tr><tr><td>Output impedance</td><td>zero</td></tr><tr><td>Slew-rate</td><td>infinite</td></tr></table> All correct 2 marks, one error 1 mark	2
	(b)	(i)	The **frequency range** over which the voltage gain is greater than $1/\sqrt{2}$ of its maximum value. (accept 0.7 or 70%)	1
		(ii)	6000 [Hz] or 6k [Hz] or 0.006 M[Hz]	1
	(c)	(i)	Horizontal line at 50 for low frequency Sloping line through (22,35)	1 1
		(ii)	12/3 = **4** V μs^{-1}	1 1
				8

Question			Marking detail	Marks available
7	(a)	(i)	16 V saturation voltage	1
		(ii)	15 / 0.2 = **75** accept other values correctly taken from graph (minus sign = 0)	1
	(b)	(i)	Feedback resistor between inverting input and output Resistor between inverting input and 0 V Microphone connected directly to non-inverting input	1 1 1
		(ii)	Resistors in the ratio 79:1 correctly assigned Both resistors $\geq 1\,\text{k}\Omega$	1 1
	(c)		16/80 = **0.200 [V]** or 200 m [V] **ecf** a (i)	1
	(d)		Both cycles show a sine wave of same phase and frequency as input. 1st cycle peak voltage of $\pm$ 12 V 2nd cycle peak voltage of $\pm$ 16 V (any clipping shown loses mark)	1 1 1
				11