GCE MARKING SCHEME

SUMMER 2017

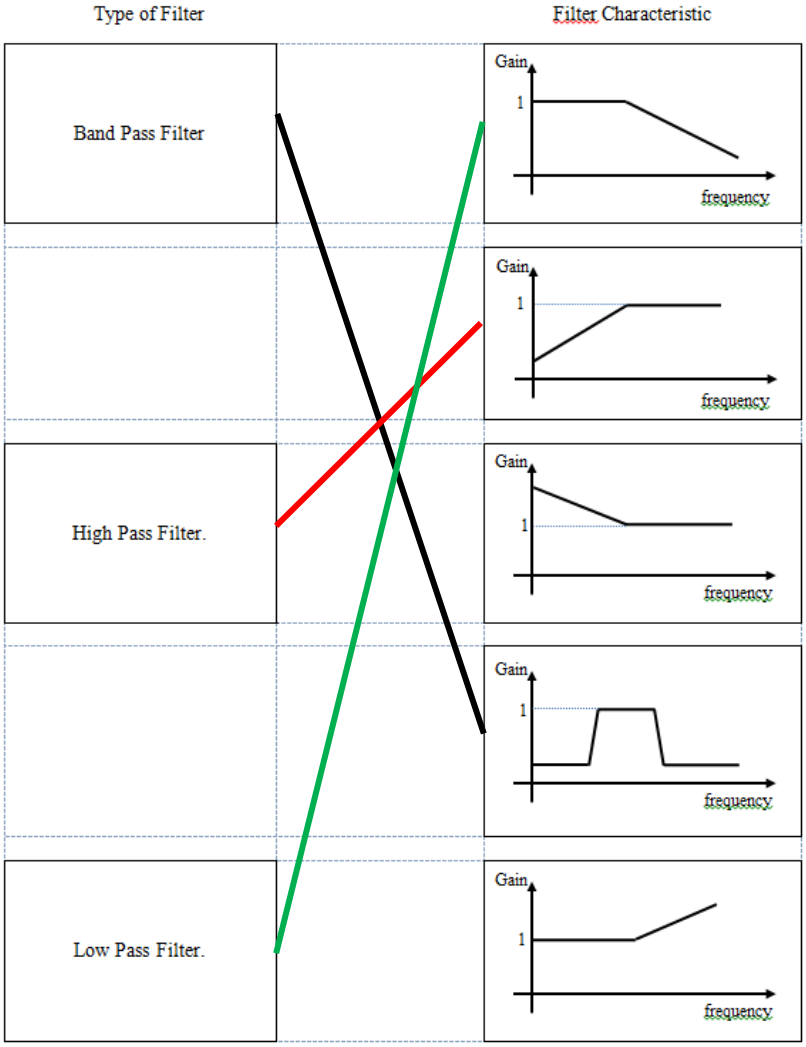
ELECTRONICS - ET4
1144/01

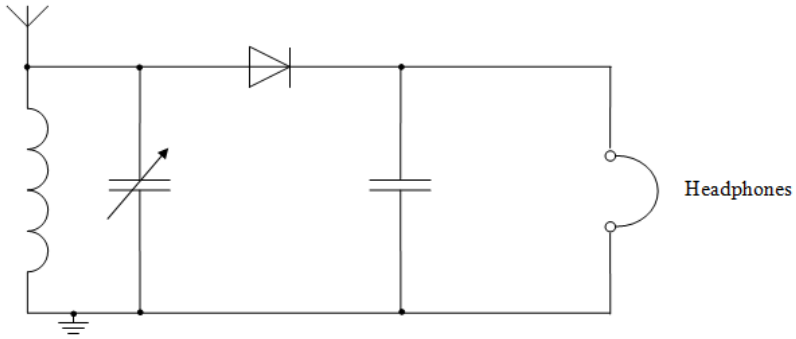
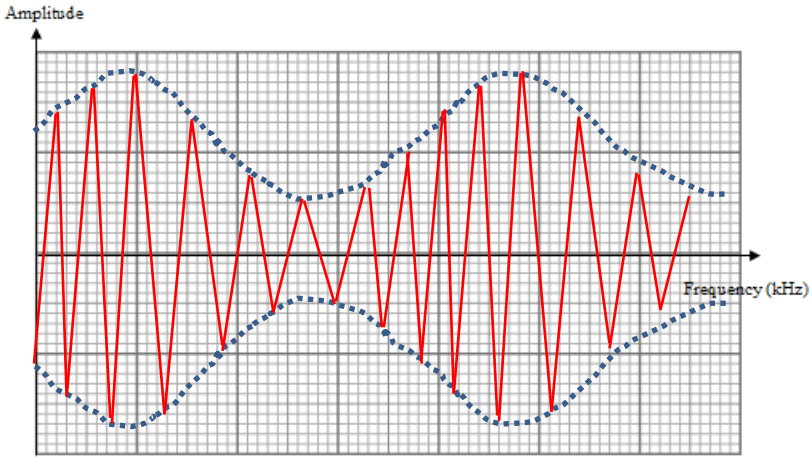
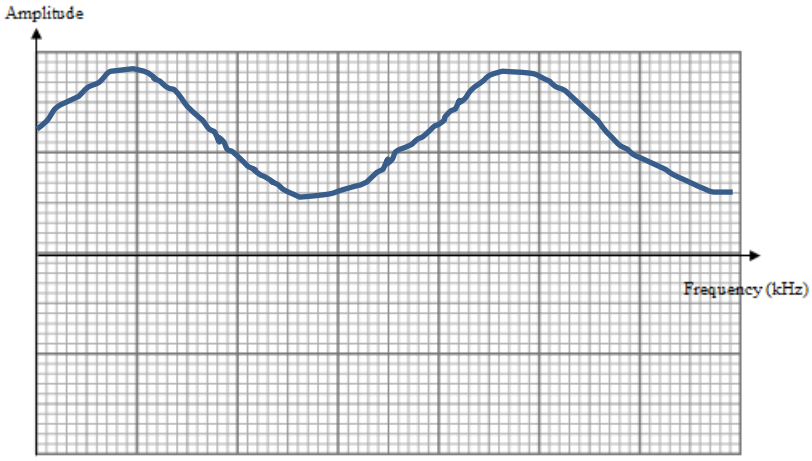
INTRODUCTION

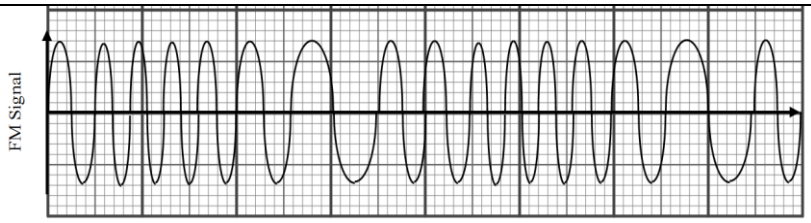
This marking scheme was used by WJEC for the 2017 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

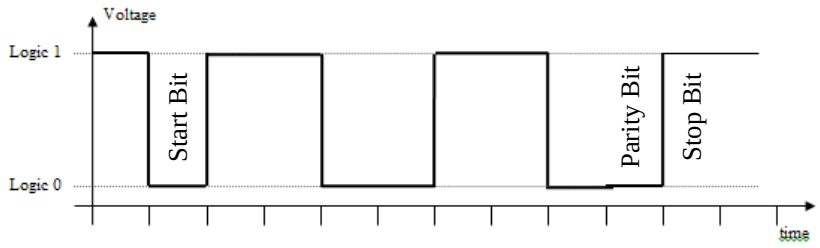
It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

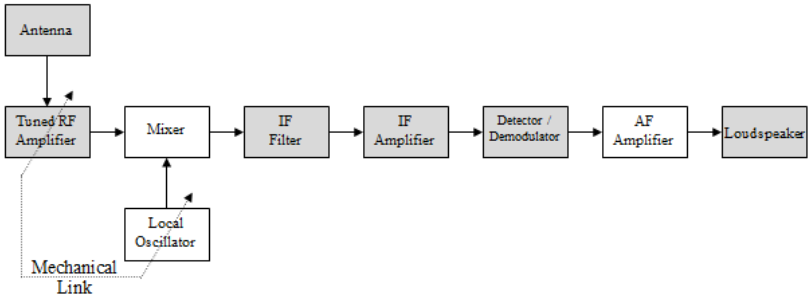
WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

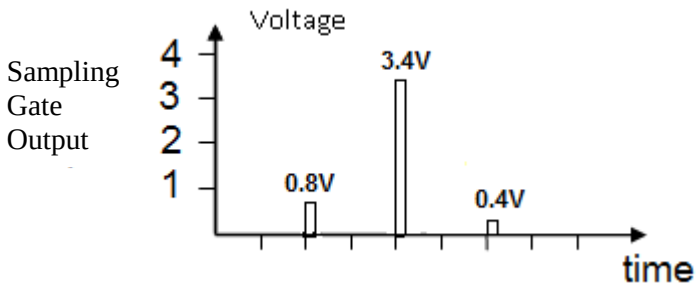
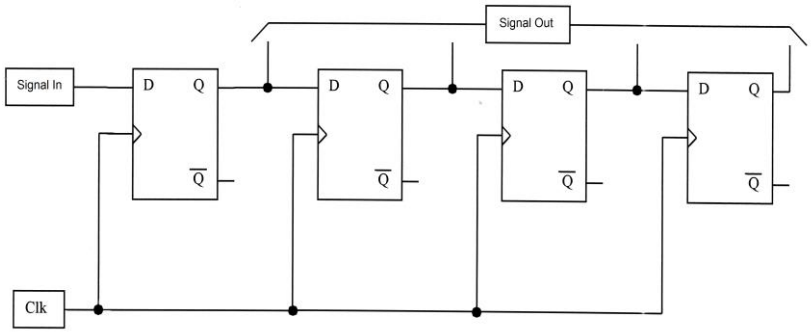
Question			Marking details	Marks Available
1				1 mark for each correct link **[3]**

Question			Marking details	Marks Available
2	*(a)*			Inductor = 1 Variable Capacitor = 1 Diode = 1 RF Capacitor = 1
	(b)	(i)		Modulated AM waveform = 1 (envelope can be shown no penalty)
		(ii)		Demodulated AM signal = 1 (with or without carrier) In phase with b(i)
				[6]

Question			Marking details	Marks Available
3.	*(a)*			Constant Amplitude = 1 Appropriate change in frequency = 1
	(b)	(i)	$\beta = \frac{\Delta f_c}{f_i}$ $\Delta f_c = \beta \times f_i = 5 \times 25 = 125 \quad kHz$	1
		(ii)	$Bandwidth = 2(\Delta f_c + f_{i(max)})$ $= 2(125 + 25)$ $= 300 \quad kHz$	1
			or	Or
			$Bandwidth = 2(1 + \beta)f_{i(max)})$ $= 2(1 + 5)25$ $= 300 \quad kHz$	1
				[4]

Question			Marking details	Marks Available
4.	*(a)*	(i)	The parity bit is a simple form of error checking. (Any reference to error correction = 0 marks)	1
		(ii)	Parity bit = 1	1
	(b)	(i)		
			All 3 labels correct or 1 label correct	2 or 1
		(ii)	3	1
	(c)	(i)	The receiving equipment would not recognise that an **even** number of errors had occurred. (Accept there are two errors)	1
		(ii)	Add additional parity bits to check on different parts of the data packet.	1 [7]
5.	*(a)*	(i)	$\frac{10 - V_{IN}}{78} = \frac{10 - 3}{56}$ $10 - V_{IN} = \frac{7 \times 78}{56}$ $10 - V_{IN} = 9.75$ $V_{IN} = 10 - 9.75 = 0.25\ \text{V}$	
			correct formula / substitution correct answer	1 1
		(ii)	$\frac{-10 - V_{IN}}{78} = \frac{-10 - 3}{56}$ $-10 - V_{IN} = \frac{78 \times -13}{56}$ $-10 - V_{IN} = -18.11$ $V_{IN} = -10 + 18.11 = 8.11\ \text{V}$	
			correct formula / substitution correct answer	1 1
	(b)		Any two from Noise, Distortion or Attenuation.	1 [5]

Question			Marking details	Marks Available
6.	*(a)*			1 mark per correct subsystem
	(b)	(i)	450kHz	1
		(ii)	Use of 0.7 max to determine bandwidth – clearly marked on graph	1
			Bandwidth = 6500Hz (accept 6000 to 6500Hz)	1
	(c)		$Q = \frac{f_o}{B} = \frac{450000}{6500} = 69.23 \cong 70$	1
	(d)		$Q = \frac{2\pi f_o L}{r_L}$ $L = \frac{Q \times r_L}{2\pi f_o} = \frac{69.23 \times 2.4}{2 \times \pi \times 450000} = 58.76\mu H$ {59.41µH if using Q=70}	Substitution / multipliers = 1 Answer = 1
	(e)		$C = \frac{1}{4\pi^2 f_o^2 L}$ $C = \frac{1}{4 \times \pi^2 \times 450000^2 \times 58.76 \times 10^{-6}} = 2.13 \times 10^{-9} = 2.13nF$ {2.08nF if using L=60µH}	Answer = 1
	(f)	(i)	$R_D = \frac{L}{r_L C} = \frac{58.76 \times 10^{-6}}{2.4 \times 2.13 \times 10^{-9}} = 11494\ \Omega$ {12500Ω if using L=60µH and C=2nF}	1
		(ii)	$I = \frac{11.6}{11494} = 1.01mA$ $R = \frac{0.4}{1.01mA} = 396\Omega$ {0.923mA, 431Ω, if R_D = 12500Ω}	Substitution / multipliers = 1 Answer = 1 **[13]**

Question			Marking details	Marks Available
7.	*(a)*		 All three levels correct – 2 marks Any one level correct – 1 mark	2
	(b)	(i)	The sampling frequency must be twice the highest frequency present in the input signal. [according to Nyquist sampling theorem]	1
		(ii)	The minimum frequency that can be used for Clock A is 38 kHz.	1
	(c)	(i)	Clock B must operate at a higher frequency than Clock A because the 12 bit output from the ADC must be output before the next sample is taken.	1
		(ii)	12 x 38kHz = 456kHz	1
	(d)		$resolution = \frac{9}{2^{12}} = \frac{9}{4096} \cong 2.197mV$ correct use of 2^{12} answer	1 1
	(e)		 Common clock Q - D x 3 Data In marked Data Out Marked	1 1 1 1
				[12]