Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A Level – LEGACY

1141/01

S18-1141-01

ELECTRONICS – ET1

MONDAY, 21 MAY 2018 – MORNING

1 hour 15 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**7**	
2.	**9**	
3.	**5**	
4.	**12**	
5.	**6**	
6.	**12**	
7.	**9**	
Total	**60**	

1141
010001

ADDITIONAL MATERIALS

A calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B+1) = A$$

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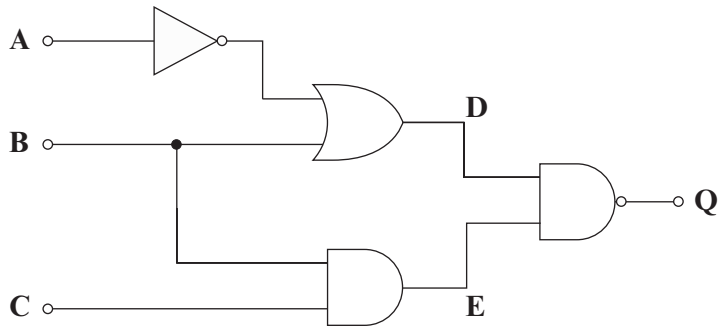
Answer **all** *questions.*

1. The following diagram shows a logic system.



(a) Write down the Boolean expressions for D, E and Q in terms of inputs A, B and C. [3]

D = ...

E = ...

Q = ...

(b) A student produces the following Boolean expression for the output of another logic system.

$Q = \overline{\overline{(A.\overline{C})} + \overline{(B + A)}}$

The teacher suggests that one of the inputs is not needed.
Apply DeMorgans theorem to this expression and simplify it to identify the input that is not needed. [4]

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Which input is not needed? .....

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2. A system of logic gates gives the following truth table.

C	B	A	P	Q
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	1	1
1	1	1	0	1

(a) (i) Use the table to write down the **unsimplified** (3 terms) Boolean expression for output P in terms of C, B and A. [1]

P = ...

(ii) Complete the Karnaugh map and determine the **simplest** expression for the output P. [3]

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C \ BA	00	01	11	10
0				
1				

P = ...

(iii) Draw the logic diagram for P using a combination of NOT, AND and OR gates. [3]

Examiner only

(b) The Boolean expression for Q is

$$Q = \overline{B} + C$$

Show how the output Q can be obtained using NAND gates. Cross out any redundant gates. [2]

Turn over.

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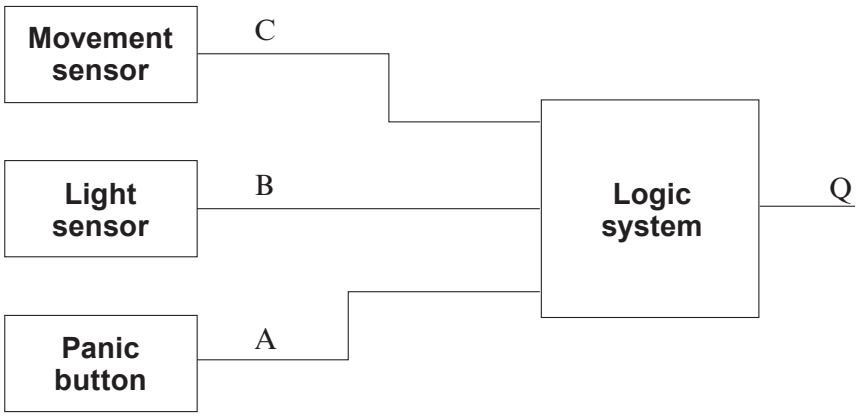
3. *(a)* A student designs a security system to switch on a floodlight when movement is detected or a panic button is pressed. The system should operate **only** when it is dark. The specifications for the sub-systems are given below:

C	Movement sensor	Movement = logic 1
B	Light sensor	Dark = logic 0
A	Panic button	Pressed = logic 1

The block diagram for the input and logic system is:



(i) Complete the truth table for the logic system such that **Q = logic 1** when the floodlight is **on**. [1]

C	B	A	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(ii) Write down the Boolean expression for Q. [1]

Q = ...

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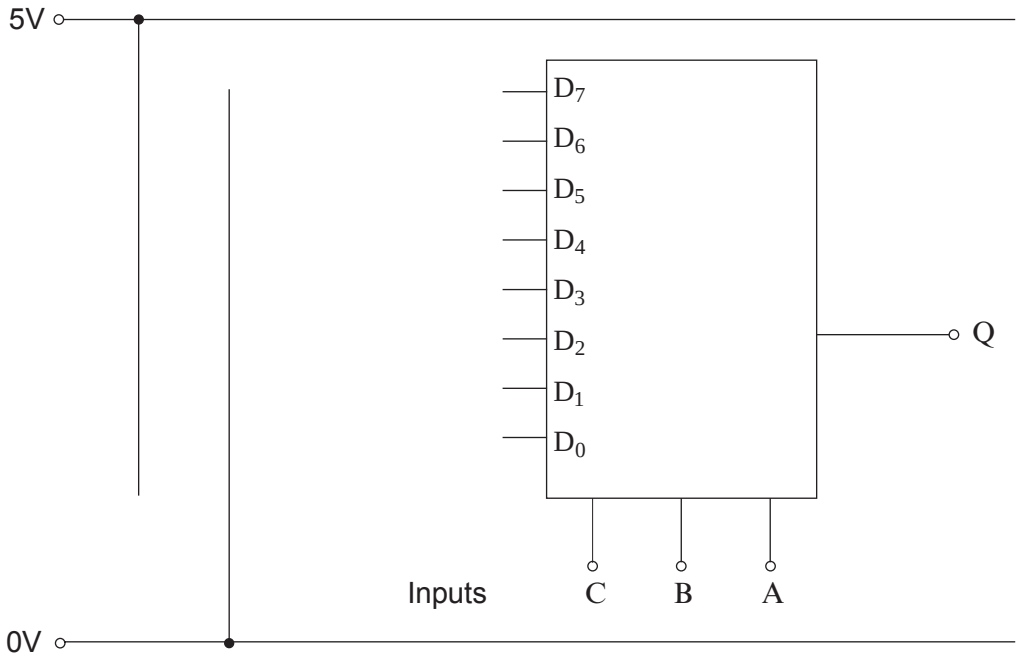
(b) Complete the diagram to show how the output Q could be generated using a multiplexer. [1]



(c) The student tests the multiplexer sub-system using a LED. Add the necessary components to the diagram so that the LED is ON when Q is high (logic 1). [2]

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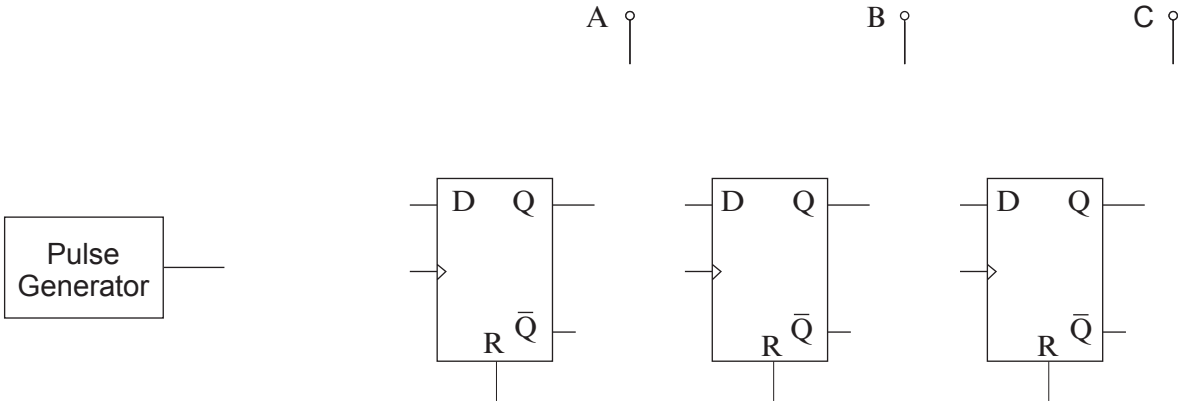
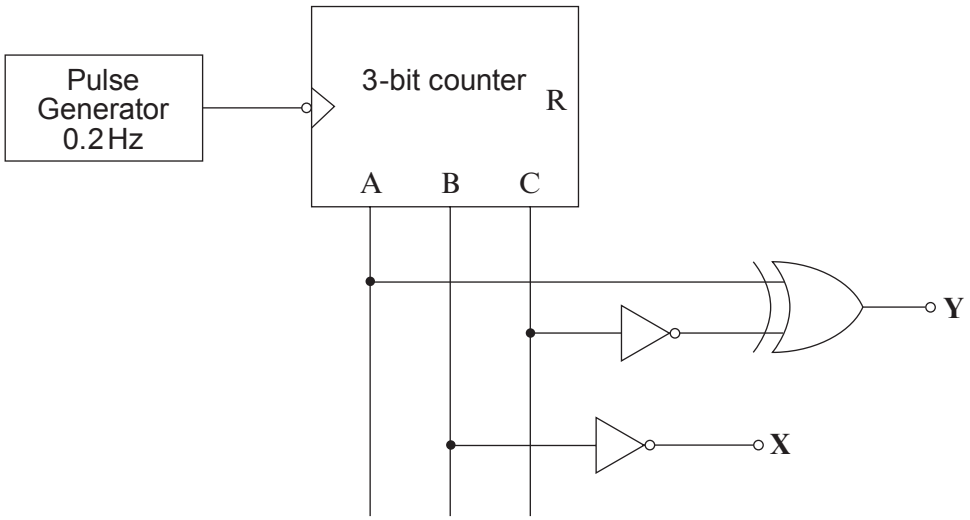
4. *(a)* Complete the diagram to make a 3 bit up-counter. [3]



(b) The following circuit uses a 3-bit **falling edge-triggered** counter.



(i) Complete the truth table for circuit. [2]

C	B	A	X	Y
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

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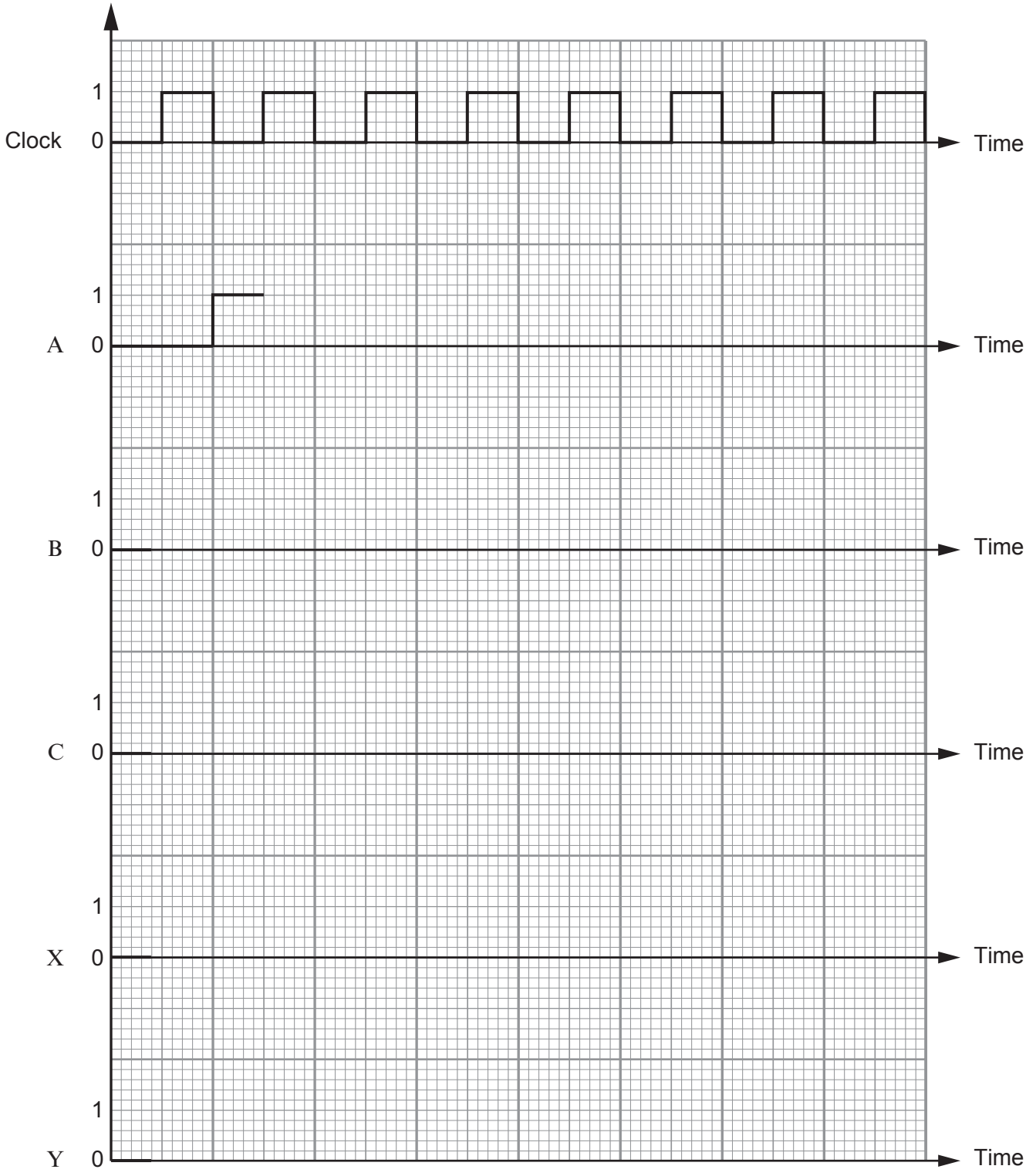
(ii) Complete the timing diagram for this system. [5]



(c) The pulse generator has a frequency of 0.2 Hz. Determine how long output C is high. [2]

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Examiner only

5. NAND gates can be used in the construction of both a transition gate and a bistable latch.

(a) What is the function of the transition gate? [1]

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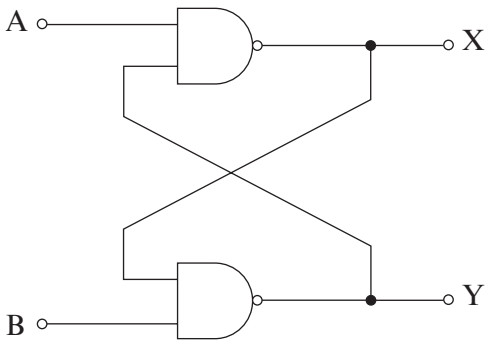
(b) In the space below draw a transition gate using 2-input NAND gates. [2]

(c) The following circuit shows a NAND gate bistable.



Complete the truth table to show the sequence of outputs at X and Y, for the given sequence of inputs. [3]

A	B	X	Y
1	1	0	1
0	1		
1	1		
1	0		
1	1		
0	0		

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6. The table shows some properties for two op-amps, S and T.

Property	S	T
Input Impedance / Ω	5×10^8	4×10^9
Open loop gain	6×10^5	1×10^6
Maximum output current / mA	5	20
Gain bandwidth product / MHz	3.6	5.0
Slew rate / $V\mu s^{-1}$	6.0	4.5
Saturation voltage / V	±18	±18

(a) (i) Explain which amplifier is capable of reaching its maximum output voltage in the **shortest** time when a large step input signal is applied. [1]

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(ii) Determine the bandwidth of amplifier S when configured to have a voltage gain of 400. [2]

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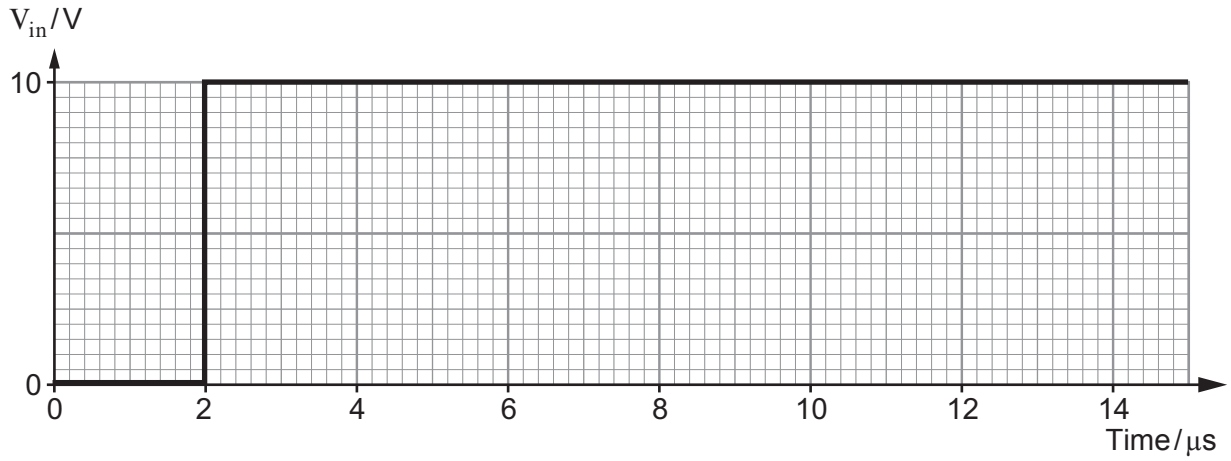
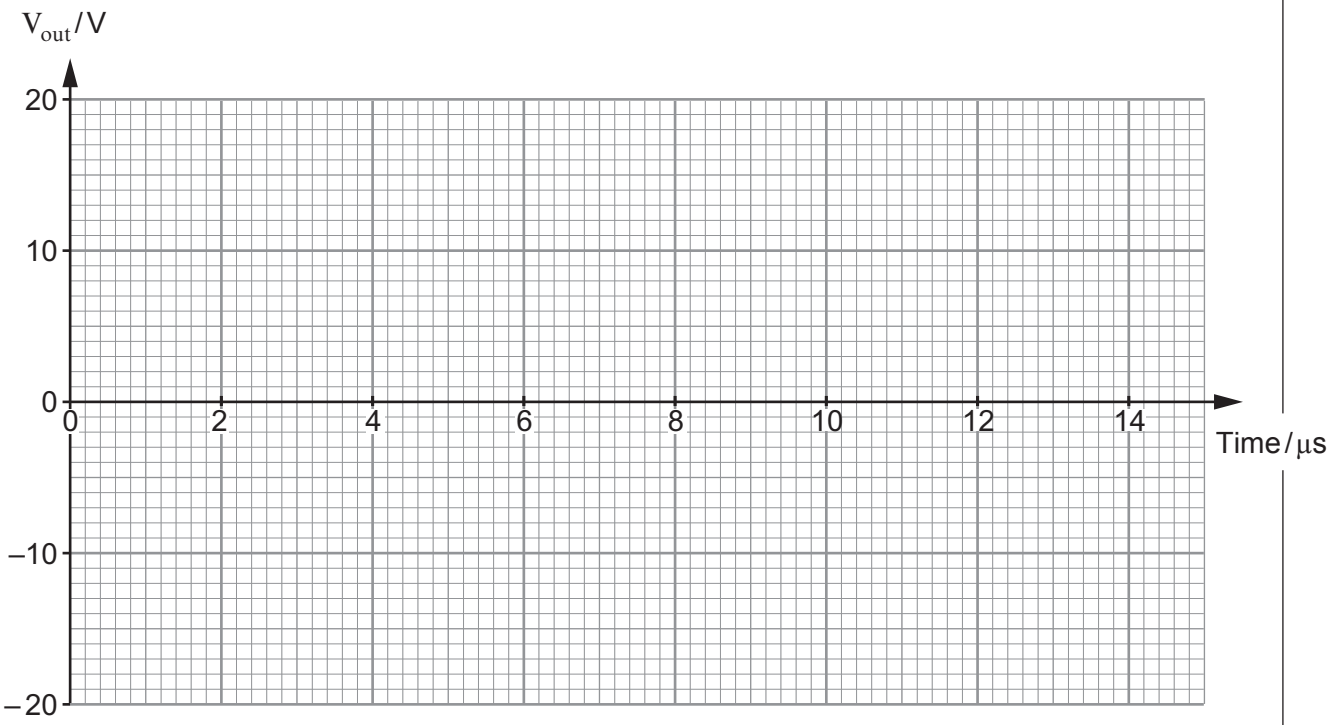
Examiner only

(b) Operational amplifier T is connected as an inverting voltage amplifier with a high gain. The following signal is applied to its input. Complete the graph to show the output voltage. The op-amp saturates at ±18 V. [3]





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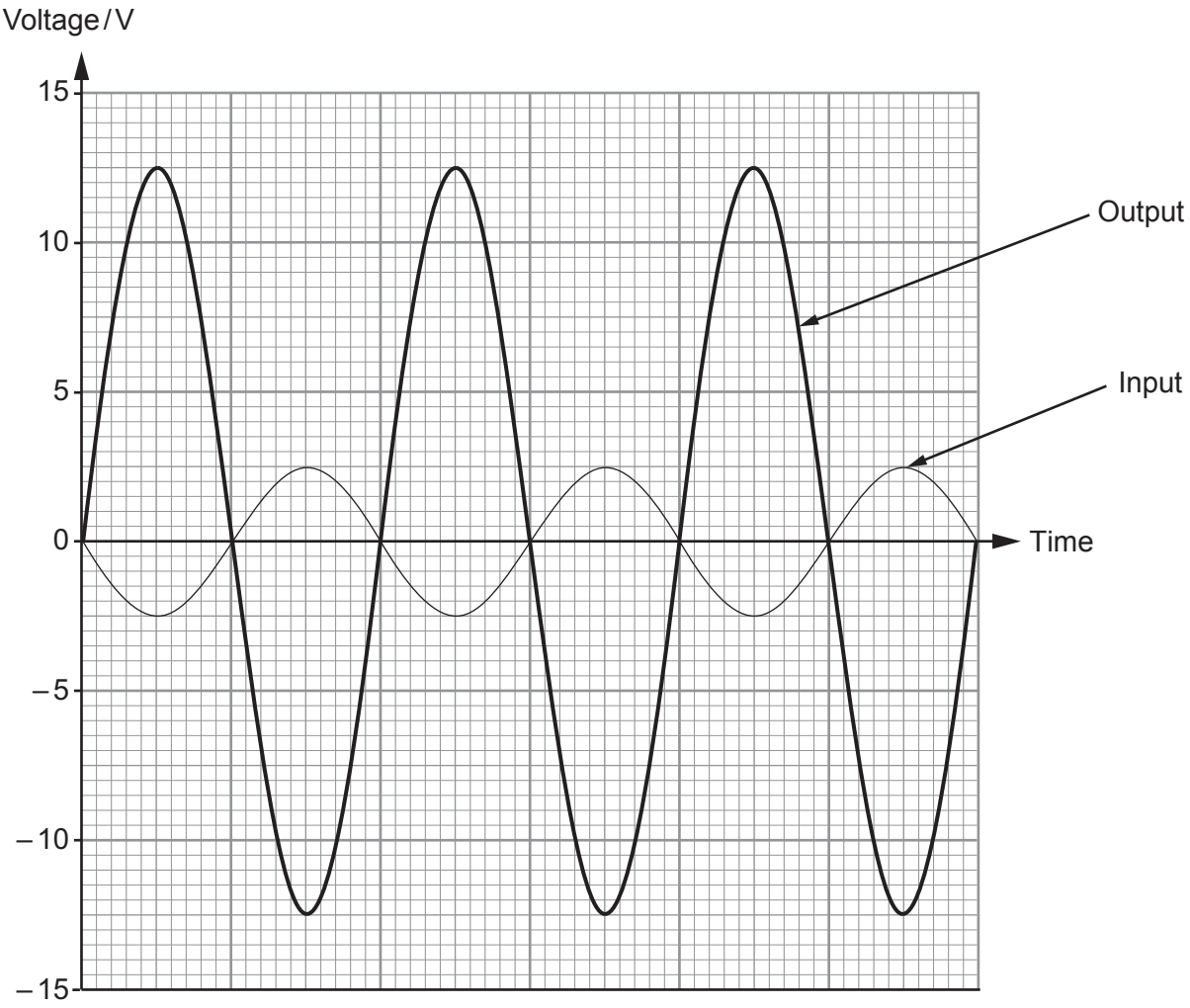
(c) Amplifier S is used to make a voltage amplifier. When tested the following input and output signals were produced.



(i) Use the graph to determine the voltage gain of the amplifier. [1]

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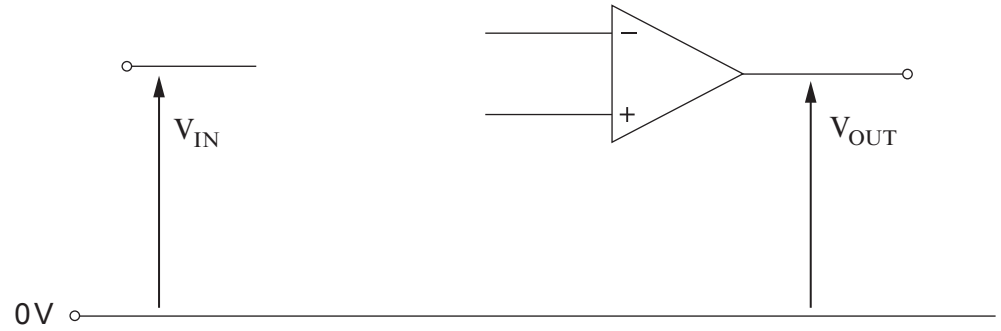
Examiner only

(ii) Complete the circuit diagram for an amplifier that would produce the graphs shown in part *(c)*(i). [3]



(iii) Determine suitable component values to produce this voltage gain and label the circuit diagram. [2]

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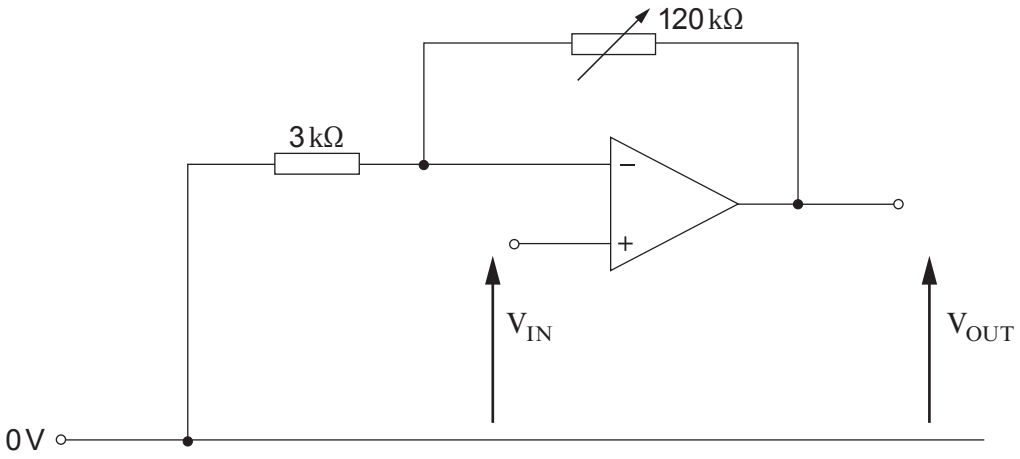
Examiner only

7. The circuit diagram shows the op-amp set up as a voltage amplifier. The variable resistor allows the user to change the gain.



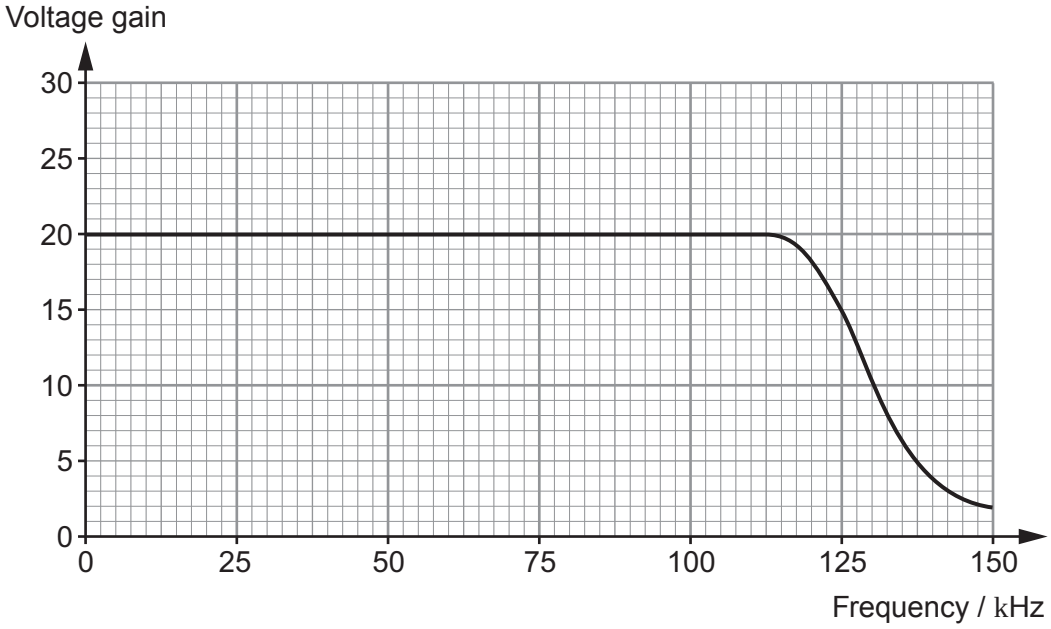
The op-amp is powered from a ±15 V supply and saturation occurs at ±14 V.

(a) Calculate the maximum and minimum voltage gain of the amplifier. [2]

Maximum gain = ...

Minimum gain = ...

The variable resistor is adjusted and the following frequency response graph is produced.



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(b) Use the graph to determine the bandwidth at this setting of the variable resistor. [2]

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(c) The variable resistor is adjusted again to give a voltage gain of 30. Determine the maximum input voltage that can be applied that avoids clipping. [2]

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(d) The variable resistor is now reduced in value. State the effect this has on: [3]

(i) The voltage gain of the amplifier.

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(ii) The input voltage at which the amplifier just saturates.

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(iii) The gain-bandwidth product of the amplifier.

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