GCE AS MARKING SCHEME

SUMMER 2018

AS
ELECTRONICS - COMPONENT 1
B490U10-1

INTRODUCTION

This marking scheme was used by WJEC for the 2018 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

WJEC Eduqas GCE AS

ELECTRONICS - COMPONENT 1

First Assessment Summer 2018

MARK SCHEME

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

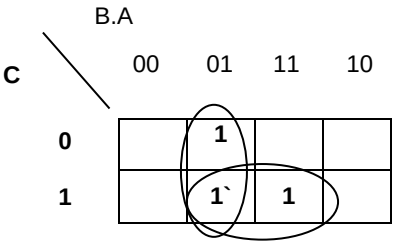
Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

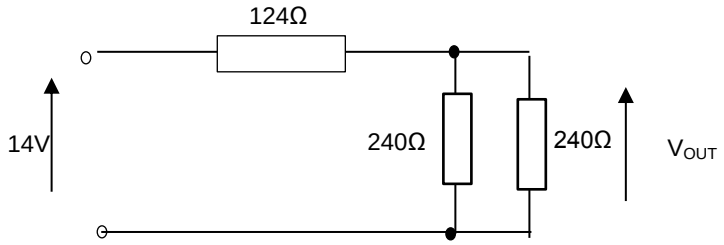
cao = correct answer only
ecf = error carried forward

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
1	*a*		<table><tr><th>B</th><th>A</th><th>X</th><th>Y</th><th>Q</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table> One mark each column correct X, Y and Q ecf Q	3			3	
	b	*i*	D_2 and D_1 connected to 5 V, D_3 and D_0 connected to 0V, others 'don't care' Allow **ecf** from table		1			
		ii	Advantage: It can be reconfigured (for a different logic function) /Fewer IC's/components needed, reprogram	1			2	
			Question 1 total	4	1	0	5	0

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	*a*	i	0 (1)	1			1	
		ii	$\bar{B}$ + A (1)	1			1	1
	b		Minimum number of groups chosen (2x4 and 1x2) (1) Any correct term from groups identified (1) Simplest overall Boolean expression (ecf) (1) C.B **+** $\overline{C}.\overline{B}$ **+** $\overline{D}$**.**$\overline{B}$**.**$\overline{A}$ *OR* *C.B* + $\overline{C}.\overline{B}$ + $\overline{D}$*.C.*$\overline{A}$	1	1 1		3	3
	c		Q = $\overline{\overline{(\bar{A}+B)}}.\bar{\bar{A}}$ or $\overline{\overline{(\bar{A}+B)}}$.A or $\overline{A.\bar{B}+\bar{A}}$ (1) = ($\bar{A}$ + B).A or $\bar{A}$ .A+ B.A (1) = B.A (1)		3		3	3
			Question 2 total	**3**	**5**	**0**	**8**	**7**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	*a*	i	Q = $\overline{C}.\overline{B}.A + C.\overline{B}.A + C.B.A$ Correct Boolean expression		1		1	1
		ii	Karnaugh method: $C.A + \overline{B}.A$ Accept $A.(C + \overline{B})$  Correct mapping (1) C.A term (1) $\overline{B}.A$ term (1) Allow error carried forward from (i) Boolean algebra method: 2 methods $\overline{B}.A(\overline{C}+C) + C.B.A$ (1) $\overline{B}.A + C.B.A$ (1) $C.A + \overline{B}.A$ or $(C + \overline{B}).A$ (1) $C.A.(\overline{B}+B) + \overline{C}\ \overline{B}.A$ (1) $C.A + \overline{C}\ \overline{B}.A$ (1) $C.A + \overline{B}.A$ or $(C + \overline{B}).A$ (1)		1 1 1		3	3
	b		NOT gate connected to B and then to AND gate with A (1) A and C to AND gate (1) Both AND gates connected to inputs of OR gate to Q (1) *(Alternative factorised solution)* *NOT gate connected to B (1)* *Output of NOT to OR gate with C (1)* *A and output of OR to AND gate (1)*	3			3	
	c		NAND gate replacement of NOT correct (1) NAND gate replacement of OR correct (1) NAND gate replacement of AND correct (1) Correct pair(s) of redundant gates crossed out (1) (apply to either solution) 2 marks MAX for incorrect connection wrt b.	3	1		4	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	*d*		Explanation identifies main functions of the flowchart. • Flow chart checks that ignition is on • If ON then delays 5s then checks if seatbelt is fastened • If seatbelt not fastened then buzzer sounds for 1s on then off for 1 s in a loop • Flowchart check seat belt at each iteration and breaks out of loop when it is fastened ie keeps buzzing until fastened.	4			4	
			Question 3 total	**10**	**5**	**0**	**15**	**4**

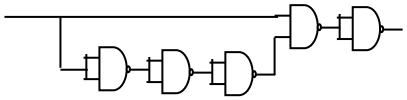
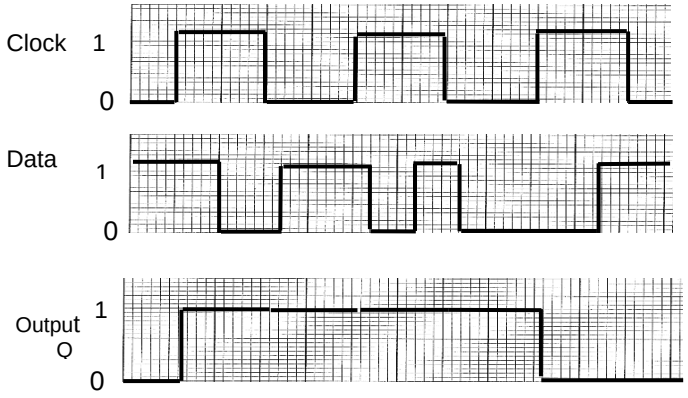
Question			Marking details		Marks available			
				AO1	AO2	AO3	Total	Maths
4	*a*		Substitution $V_{OC} = V_{IN}\, R_2/(R_1 + R_2)$ = 18 x 560/(160 + 560) (1) = 14V (1) Or $I = (V_{IN}/R_1 + R_2)$ and $V_{OC} = IR_2$ I_{SC} = 18/160 = 0.1125A (1) R_o = 14/0.1125 = 124.4Ω (1) ecf V_{OC}, I_{SC}	1	1 1 1		4	4
	b	i	Correctly drawn equivalent circuit with parallel load (1) All values labelled on diagram (1)  	1 1				
		ii	Parallel resistance calculated as 120Ω (1) (can be implied in working) Substitution $V_{OUT} = V_{IN}\, R_2/(R_1 + R_2)$ = 14 x 120/(124 + 120) (1) = 6.9 V (1) Or I=14/244 =0.057A (1) V_{OUT} =0.057x120 =6.9V (1)	1	1 1		5	2
			Question 4 total	**4**	**5**	**0**	**9**	**6**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	*a*		**Indicative Content:** **AO2 content:** applies knowledge of input and output subsystems, logic systems and semiconductor components. **AO3 content:** analyses a problem, and evaluates an electronic system to meet a given specification. Designs improvements to fully meet the specification The voltage at A goes from low in the light to high in the dark. However, the switching of the logic gate will be subject to minor fluctuations in light intensity and so a Schmitt inverter at A would provide suitable signal conditioning to eliminate this effect. This would then require the LDR and the 10k resistor to be interchanged to produce the logic 1 at the input of the OR gate when the beam is broken. (If other photosensitive devices are suggested these must be correctly integrated into the circuit and their use justified). The diode on the output stage needs to be in parallel with the solenoid and reverse biased to prevent adverse effects causes by back-emf. 5-6 marks Addresses each bullet point in the specification. Identifies the issues outlined above and the problems that they introduce. Proposes correct ways of remedying them. *There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.*		2	4	6	

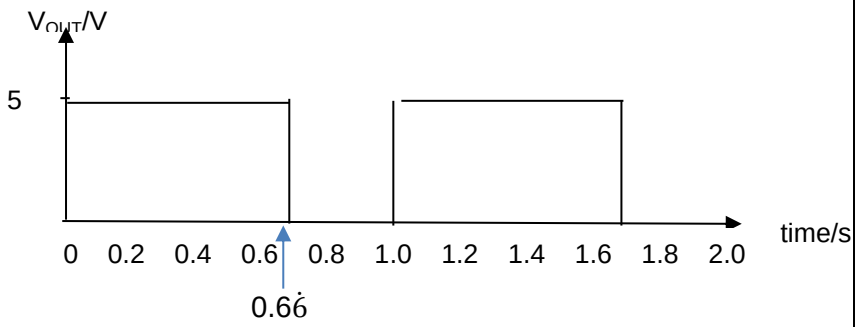
			3-4 marks Compares the specification and the design, identified some potential problems and gives an indication of how these may effect the working of the system. Some attempt made to rectify these design flaws. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information that is not relevant to the argument.* **1-2 marks** One problem associated with the given design identified and corrected *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.* **0 marks** *No attempt made or no response worthy of credit*.					

				AO1	**AO2**	**AO3**	**Total**	**Maths**
5	*b*	i	$I_C = h_{FE}I_B$ I_B =200/80 = 2.5 mA (1) V_R = 11.6 – 0.7 = 10.9V (1) R = V/I = 10.9/ 2.5 x 10^{-3} = 4360 [Ω] accept 4.4 kΩ (1) ecf I_C/R	1	1 1 1		4	2
		ii	Preferred resistor is nearest value **below** that calculated in (i) e.g. 4300Ω					
			Question 5 total	**1**	**5**	**4**	**10**	**2**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	*a*	i	R_T = 5kΩ ± o.1 kΩ Substitution $V_T = V_{IN}\, R_2/(R_1 + R_2)$ = 12 x 5/(10 + 5) (1) = 4 V (1) ecf R_T	1	1 1		3	3
		ii	Use of potential divider formula or ratio method (1) R_V = 30 kΩ (1)	1	1		2	2
	b		At 20°C $V_T > V_X$ (1) therefore $V_{OUT} \approx$ 12V (1) As temperature goes above 25°C V_T decreases until it falls below V_X (4V) (1) therefore $V_{OUT} \approx$ 0V (1)		4		4	
	c		Heater connected between 12V and Drain of MOSFET (1) Comparator connected to Gate and Source connected to 0V (1) Award 1 mark for voltage follower circuit	1 1			2	
	d	i	substitution into P = IV 48 = I x 12 I = 4 [A] (1) substitution into $I_D = g_m(V_{GS}-3) \therefore g_m = 4/(12-3)$ (1) g_m = 0.44 [S] (1) ecf I (Use of 60W hence 5A apply ecf for 2nd and 3rd marks) i.e. $g_m = 5/(12-3)$ (1) g_m = 0.56 [S]	1 1	1		3	3
		ii	Selection and substitution $P = I^2R$ $P = 4^2$ x 0.08 (1) P = 1.28 W (1) ecf 5A from d(i) $P = 5^2$ x 0.08 (1) P = 2.0 W (1)	1	1		2	2
			Question 6 total	**7**	**9**	**0**	**16**	**10**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7	*a*		<table><tr><td>A</td><td>B</td><td>X</td><td>Y</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>**1**</td><td>**0**</td></tr><tr><td>1</td><td>1</td><td>**1**</td><td>**0**</td></tr><tr><td>1</td><td>0</td><td>**0**</td><td>**1**</td></tr><tr><td>1</td><td>1</td><td>**0**</td><td>**1**</td></tr><tr><td>0</td><td>0</td><td>**1**</td><td>**1**</td></tr></table>				3	3
				Setting/resetting correct (lines 2+4) (1) Latching correct (lines 3+5) (1) Forbidden combination (line 6) (1)				
	b		Propagation delay is the time taken for the output to respond to a change in input (1) 3 NANDS connected as NOT gates in series (1) Connected as shown to 4th NAND gate (1) 5th NAND gate used (1) 	1 1 1 1			4	
	c		 Q rises on 1st clock rising edge. (1) Q falls on 3rd clock rising edge. Provided no intermediate pulse (1) $\overline{Q}$ is INVERSE of Q (1)		3			
			Question 7 total	**7**	**3**	**0**	**10**	**3**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8	*a*		V_{OUT} = - 40(2/20 + 1.8/10) (1) V_{OUT}= -11.2 V (1)	1	 1		2	2
	b		V_{OUT} is an inverted sine wave of same frequency (1) Amplitude 4V (1) Offset by -4V (between 0 and -8) (1)	1	 1 1		3	2
			Question 8 total	**2**	**3**	**0**	**5**	**4**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9	*a*	i	C =1.44/(R_1 + 2R_2) x f select and rearrange formula (1) C = 1.44/(30 + 60)x10^3 x1 = 1.44/90x10^3 (1) substitution = 16x10^{-6} or 16µF (1)	1 1	0 1		3	3
		ii	Substitute t_H/t_L =0.7x(30+30)C/0.7x30xC = 2:1	1	 1		2	2
		iii	 2 cycles of an astable with T=1s (1) Correct mark/space ratio ecf a(ii) (1)	 1	 1		 2	1
	b		All $\bar{Q}$'s to D's (1) Then either: Pulses In to clock A then all $\bar{Q}$'s used to propagate signal (1) i.e.to subsequent clock inputs All Q's to output flags (1) Or Pulses In to clock A then all Q's used to propagate signal (1) i.e.to subsequent clock inputs All $\bar{Q}$ to outputs flags (1)	1 1 1			3	
	c	i	A and D to inputs of AND gate P Output of P to R		1 1		2	

<table>
<tr>
<td>9</td><td>c</td><td>ii</td>
<td>
<table>
<tr><th>Clock Pulse</th><th>D</th><th>C</th><th>B</th><th>A</th><th>X</th><th>Y</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>9</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table>

One mark for each correct column X and Y (rows 0-8) (2)
Line for clock pulse 9 same as line zero (wrt answer in table) (1)
</td>
<td></td><td>3</td><td></td><td>3</td><td>3</td>
</tr>
<tr>
<td></td><td>d</td><td></td>
<td>X ON for 6 seconds (1) then
X OFF for 2 seconds (1)
ecf table</td>
<td></td><td>1
1</td><td></td><td>2</td><td></td>
</tr>
<tr>
<td></td><td></td><td></td>
<td>Question 9 total</td>
<td>7</td><td>10</td><td>0</td><td>17</td><td>9</td>
</tr>
</table>

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
10	*a*		4 diodes arranged as a bridge (correct orientation of diodes) (1) Correct connections of transformer to bridge (1) Correct connections of bridge to circuit (1)	3			3	
	b		$V_{PEAK} = 8.5x\sqrt{2}$ (1) correct rearrangement and substitution $= 12$ V (1) $V_1 = 12 - 1.4 = 10.6$V (1) ecf V_{PEAK}	1	 1 1		3	2
	c		Graph with 4 positive sinusoidal pulses (1) Voltage labelled showing peaks at 10.6V (1) Or 12V peak labelled, 10.6 by eye	1	 1		2	2
	d		Graph showing ripple voltage (1) Voltage peaks at 10.6V (1)	1	 1		2	1
	e		5.6V Zener diode (correct position and orientation)…. (1) …forms potential divider with a resistor across the rails (1) Load resistor R across zener (1)	1 1 1			3	
			Question 10 total	**9**	**4**	**0**	**13**	**5**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
11	*a*		Identifies the need to design a non-inverting amplifier (1) with a gain of +24 from analysis of graph (1) (Voltage gain = 1200/50 =24 ignore any unit) Resistor (R_f) between output and inverting input (1) Resistor (R_1) between inverting input and 0V (1) Input signal directly to non-inverting input (1) Resistor values in correct ratio: $R_f = 23x\ R_{IN}$ (1) *If inverting amp drawn with resistors giving gain of 24 then 2 marks: R_f connection (1) Ratio 24:1 (1)* (ecf to voltage gain stated above) (Both resistor values ≥ 1kΩ)			1 1 1 1 1 1	6	1 1
	b		**Indicative Content:** **A01 allocation -** Two types of distortion are clipping distortion and distortion that occurs when the slew-rate of the op-amp is exceeded. **A03 allocation -** Clipping distortion occurs because the power supply requirements limit the output voltage swing. Typically, op-amps have a saturation voltage a fraction of a volt below the power supply output. If the voltage gain of the amplifier is such that the calculated peak output voltage exceeds the saturation value, then the output voltage flattens out. Any of the following will reduce or eliminated this effect; increase the power supply voltage, reduce the gain of the amplifier or reduce the input voltage. Slew rate is the maximum rate that the output voltage can change (w.r.t. time). It is a parameter of the particular op- amp. If the frequency or amplitude of the input signal is too high the output will become distorted and will appear as a ramp (saw-tooth) of fixed gradient. Reduce the effect by using an op-amp with a higher slew-rate or reducing the frequency or amplitude of the input signal where possible	1		5	6	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
11	*b*		**5 – 6 marks** Identifies two types of distortion with a good explanation of how each is caused and/or uses diagrams to show the effect of each on the output signal. Details of how to reduce both effects are included in the argument: *There is a sustained line of reasoning which is coherent, relevant, substantiated and logically structured. The information included in the response is relevant to the argument.* **3 – 4 marks** Identifies two types of distortion with a reasonable explanation of how they are caused and/or uses diagrams to show the effect on the output signal. Some reference made to how to reduce the effects: OR Good explanation of at least one type of distortion and its cause and effect on the output signal and an explanation of how to reduce its effect. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information that is not relevant to the argument.* **1 -2 marks** One type of distortion identified with partial explanation and/or uses diagrams to show the effect on the output signal. *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.* **0 marks** *No attempt made or no response worthy of credit.*					
			Question 11 total	**1**	**0**	**11**	**12**	**2**

COMPONENT 1

SUMMARY OF MARKS ALLOCATED TO ASSESSMENT OBJECTIVES

Question	AO1	AO2	AO3	TOTAL MARK	MATHS
1	4	1	0	5	0
2	3	5	0	8	7
3	4	5	0	9	6
4	10	5	0	15	4
5	1	5	4	10	2
6	7	9	0	16	10
7	7	3	0	10	3
8	2	3	0	5	4
9	7	10	0	17	9
10	9	4	0	13	5
11	1	0	11	12	2
TOTAL	**55**	**50**	**15**	**120**	**52**