GCE MARKING SCHEME

SUMMER 2018

GCE (LEGACY)
ELECTRONICS - ET1
1141/1

INTRODUCTION

This marking scheme was used by WJEC for the 2018 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

GCE (LEGACY)

ELECTRONICS - ET1

SUMMER 2018 MARK SCHEME

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>1.</td><td>(a)</td><td></td><td>D = B + $\overline{A}$
E = C.B
Q = $\overline{C.B.(B+\overline{A})}$ or $\overline{(B+\overline{A})}$ + $\overline{C.B}$ or $\overline{B}$.A + $\overline{C.B}$
($\overline{C.B}$ can be replaced by $\overline{C}$ +$\overline{B}$ in either alternative answer)</td><td>1
1
1</td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>(A.$\overline{C}$).(B + A) DeMorgan's theorem correctly applied
Allow double bar over each term
A.B.$\overline{C}$ + A.$\overline{C}$ allow A.B.$\overline{C}$ + A.$\overline{C}$.A
A.$\overline{C}$(B + 1) either or both simplifications
A.$\overline{C}$ Simplest expression stated

Input B is redundant (mark can only be awarded if results from correct analysis)</td><td>1
1
1

1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>7</td></tr>
<tr><td>2.</td><td>(a)</td><td>(i)

(ii)</td><td>P = $\overline{C}$.B.$\overline{A}$ + C.$\overline{B}$.$\overline{A}$ + C.B.$\overline{A}$

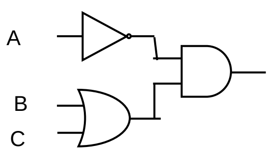
<table><tr><th>C \ BA</th><th>00</th><th>01</th><th>11</th><th>10</th></tr><tr><td>0</td><td></td><td></td><td></td><td>1</td></tr><tr><td>1</td><td>1</td><td></td><td></td><td>1</td></tr></table>
Correct transfe[illegible]ta to Karnaugh map

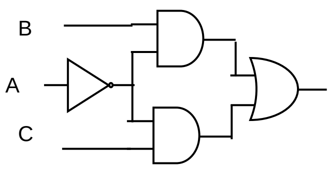
P = B.$\overline{A}$ + C.$\overline{A}$ or P = $\overline{A}$.(B + C)
1 mark for each correctly identified group from table drawn (max. 2)</td><td>1

1

2</td></tr>
<tr><td></td><td></td><td>(iii)</td><td>Input A connected to input of NOT gate.
Then either
Inputs B and C connected in inputs of OR gate
Outputs of NOT and OR connected to P using AND gate

OR
Inputs B and C each to a separate AND gate with output of NOT A
Outputs of AND gates to P via an OR gate

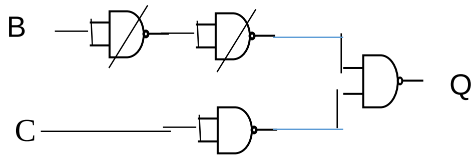



</td><td>1

1
1

OR
1

1</td></tr>
</table>

Question			Marking detail	Marks available
	(b)		 Input B shown with redundant gates or as a direct connection to final NAND gate. Input C connected through NAND invertor to final NAND gate.	 1 1
				9

Question			Marking detail	Marks available
3.	(a)	(i)	<table><tr><th>C</th><th>B</th><th>A</th><th>**Q**</th></tr><tr><td>0</td><td>0</td><td>0</td><td>**0**</td></tr><tr><td>0</td><td>0</td><td>1</td><td>**1**</td></tr><tr><td>0</td><td>1</td><td>0</td><td>**0**</td></tr><tr><td>0</td><td>1</td><td>1</td><td>**0**</td></tr><tr><td>1</td><td>0</td><td>0</td><td>**1**</td></tr><tr><td>1</td><td>0</td><td>1</td><td>**1**</td></tr><tr><td>1</td><td>1</td><td>0</td><td>**0**</td></tr><tr><td>1</td><td>1</td><td>1</td><td>**0**</td></tr></table>	
			Column Q correct	1
		(ii)	Q = $\overline{C}.\overline{B}.A + C.\overline{B}.\overline{A} + C.\overline{B}.A$ or $C.\overline{B} + \overline{B}.A$ or $\overline{B}.(C + A)$	1
	(b)		D_0, D_2, D_3, D_6 and D_7 to 0 V D_1, D_4, and D_5 to 5 V Completely correct 1 mark (allow ecf from (a))	1
	(c)		LED (correct orientation) and series resistor connected between power rail and Q	1
			Between Q and 0 V	1
				5

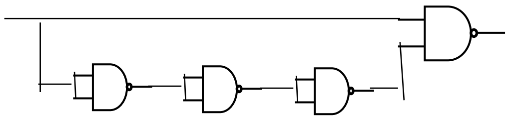
<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>4.</td><td>(a)</td><td></td><td>All 3 clock inputs correctly connected
$\overline{Q}$ outputs to D (all 3 correct)
Q outputs to correct terminals</td><td>1
1
1</td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td><table><tr><th>C</th><th>B</th><th>A</th><th>X</th><th>Y</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr></table>One mark each correct column X and Y</td><td>2</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>A pulses twice clock duration starting on the first falling edge of the clock.
Both pulses B and C correct duration
Both pulses B and C correct timing.
X inverse of B
Y logic 1 for first two spaces of A and then logic 1 for last two pulses of A. Allow bod if X or Y starting from first falling edge of A.
(X and Y ecf from table)</td><td>1

1
1
1
1</td></tr>
<tr><td></td><td>(c)</td><td></td><td>Convert frequency to time period using T=1/f = 1/0.2 =5 s
C has a duration of 4 pulses. 4x5 = 20 s</td><td>1
1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>12</td></tr>
</table>

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>5</td><td>(a)

(b)

(c)</td><td></td><td>The transition gate produces edge-triggering /produces a <u>very short</u> pulse.

An odd number of NAND's as series NOT gates
Correct connections to the final NAND gate (Final NAND invertor is neutral)
e.g.

<table>
<tr><th>A</th><th>B</th><th>X</th><th>Y</th></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table>
X has correct response to SET (when A=0 initially)
Y has correct response to RESET (when B=0 initially)
(mark for 1st four lines only)
Correct last line</td><td>1

1
1

1
1

1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>6</td></tr>
<tr><td>6.</td><td>(a)</td><td>(i)</td><td>S (no mark) '<u>as it has the higher slew rate'</u>
(or both time calculations shown)</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>$3.6 \times 10^6/400$ (correct substitution and re-arrangement)
9000 (Hz) or 9 k(Hz) or 0.009 M(Hz)</td><td>1
1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>Downward sloping line starting at 2 µs
Correct gradient (passes through 4,-9)
Saturates at -18 V</td><td>1
1
1</td></tr>
<tr><td></td><td>(c)</td><td>(i)</td><td>12.5/2.5 = (-) 5</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Resistor connected between output and inverting input
Resistor connected between V_{IN} and inverting input
Non-inverting input connected to 0 V (NIA = 1 mark)</td><td>1
1
1</td></tr>
<tr><td></td><td></td><td>(iii)</td><td>Ratio R_F/R_{IN} = 5 and both 1 kΩ or greater (ecf (i) and (ii))
Clearly labelled on diagram (accept in written answer if unambiguous). Full credit for NIA values if correct wrt earlier parts.</td><td>1
1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>12</td></tr>
</table>

Question			Marking detail	Marks available
7.	(a)		Max. gain = 41 Min. gain = 1	1 1
	(b)		Bandwidth measured at $20/\sqrt{2}$ or 0.7x 20 ($\cong 14$) (indicated on graph or implied) 125 (kHz) range 125-127	1 1
	(c)		14/30 or 14000/30 (correct substitution) $0.46\dot{6}$ or $0.4\dot{6}$ or $0.46\dot{6}$ mV (rounded-up answers e.g. 0.467 award 1-mark total as this will go over saturation voltage)	1 1
	(d)	(i)	Voltage gain **reduces**	1
		(ii)	Input voltage **increases**	1
		(iii)	Gain- bandwidth product **remains constant / unchanged**	1
				9