GCE MARKING SCHEME

SUMMER 2018

GCE (LEGACY)
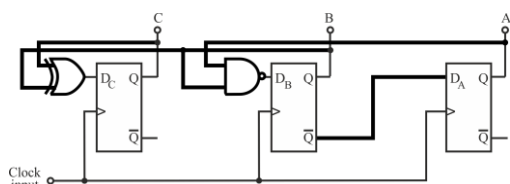**ELECTRONICS - ET5**
1145/1

INTRODUCTION

This marking scheme was used by WJEC for the 2018 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

1. *(a)*

D_A correct	1 mark
Use of $\overline{Q_B}$	1 mark
D_B correct	1 mark
D_C correct	1 mark

(b) (i)

Clock pulse	Current Outputs			Next Outputs		
	C	**B**	**A**	D_C	D_B	D_A
1	0	1	1	**1**	**0**	**0**
2	**1**	**0**	**0**	1	1	1

Correct transition for clock pulse 1	1 mark
Correct transition for clock pulse 2	1 mark
Type of state = **main sequence**	1 mark

(ii)

Clock pulse	Current Outputs			Next Outputs		
	C	**B**	**A**	D_C	D_B	D_A
1	0	1	0	**1**	**1**	**0**
2	**1**	**1**	**0**	0	1	0

Correct transition for clock pulse 1	1 mark
Correct transition for clock pulse 2	1 mark
Type of state = **stuck**	1 mark

(iii)

Clock pulse	Current Outputs			Next Outputs		
	C	**B**	**A**	D_C	D_B	D_A
1	0	0	1	**0**	**1**	**1**
2	**0**	**1**	**1**	1	0	0

Total for Q1   7

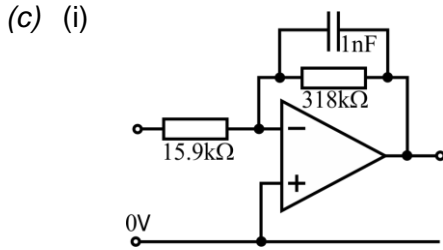|	
Correct transition for clock pulse 1	1 mark
Correct transition for clock pulse 2	1 mark
Type of state = **unused**	1 mark

Total for Q1   13

2. *(a)* **Bass boost filter** — 1 mark

(b) (i) **Treble cut filter** — 1 mark

(ii) Break frequency = **500**Hz — 1 mark

(iii) Frequency = **200**Hz — 1 mark
Amplitude = **400**mV — 1 mark

(iv) Active because **low frequency gain >1** (or equivalent) — 1 mark

(c) (i)

Capacitor in parallel with a resistor — 1 mark
Capacitor in feedback circuit — 1 mark
Rest of circuit correct — 1 mark

(ii) Use of break frequency formula to give
feedback resistor value between **318** kΩ and **319** kΩ — 1 mark
Use of voltage gain formula to give
input resistor value between **15** kΩ and **16** kΩ — 1 mark
Evidence of correct interpretation of multipliers 'k' and 'n' in either calculation — 1 mark
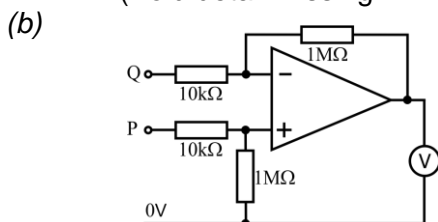In (c), allow ecf throughout.

Total for Q2	**12**

3. *(a)* (i) Voltage at Q = **5.92**V (or implied) (accept 5.91 but not 5.9) — 1 mark
Voltmeter reading = **0.08**V (accept 0.09 but not 0.1) — 1 mark

(ii)
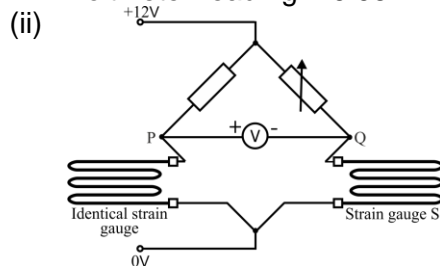
Correct circuit diagram — 1 mark
Second strain gauge must **negate effect of temperature change** and **not subject to strain (or equivalent)** — 2 marks
(Bold detail missing - 1 mark only)

(b)

(i) Circuit diagram correct — 1 mark
Correct ratio of resistors (Feedback:Input = 100:1) — 1 mark
All resistor values correct and labelled — 1 mark

(ii) Labels P and Q correct — 1 mark

(iii) Voltmeter reading = 100 x 0.08 = **8**V (allow ecf from (a)(i) and (ii)) — 1 mark

Total for Q3	**10**

2

4. *(a)* **Ensures rapid response - if polled in the main program, response could take 20s** (or equivalent)   1 mark

(b) movlw   b'**10010X0X**' ('X' = don't care)

            interrupts enabled correctly   (5 msb correct)   1 mark

            INTF cleared   (3 lsb correct)   1 mark

(c) (i)

201 inter	movwf	store	
202	bcf	INTCON,1	
203 loop	**movlw**	**b'01010'**	
204	movwf	PORTA	
205	**call**	**threesec**	
206	**movlw**	**b'10101'**	
207	movwf	PORTA	
208	call	threesec	
209	btfss	PORTB,2	
210	goto	loop	
211	movf	store	
212	retfie		

Line 203 correct   1 mark
Line 205 correct   1 mark
Line 206 correct   1 mark
(accept **b'10101'** for 203 **AND b'01010'** for 206)

(ii) Working register contains b'**00001010**'   accept decimal 10   1 mark
(iii) Working register contains b'**00001111**'   accept decimal 15   1 mark
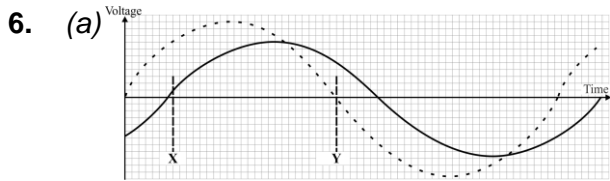
                                                Total for Q4   8

5. *(a)* $R_B = $ **80** kΩ
        $R_C = $ **40** kΩ

                           Both correct   1 mark

(b) $V_{dac} = $ **-1.0**V   1 mark

(c)   Max. $V_{dac} = $ **-15.0**V (allow ecf, i.e. (c) = 15 x (b))   1 mark
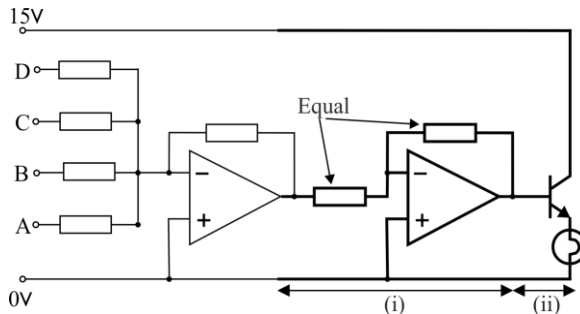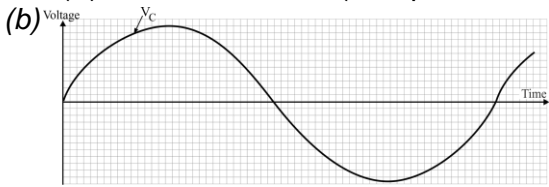

(i) Correct circuit diagram for inverting amp.   1 mark
    Equal resistors > 1 kΩ 1 mark
(ii) Lamp connected from emitter to 0V   1 mark
    Rest of emitter follower circuit correct   1 mark
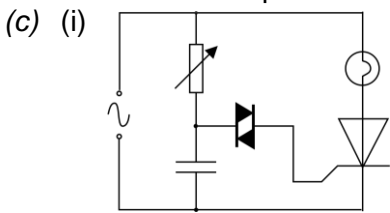   (1 mark only for (ii) if lamp is in collector circuit.)

                                                  Total for Q5   7

6. *(a)*

(i)	X correct	1 mark
(ii)	Y correct	1 mark
(iii)	7/62 x 360 = **35⁰** (accept 30⁰ to 40⁰)	1 mark

(b)

Correct phase	1 mark
Correct amplitude	1 mark

(c) (i)

|		
	Correct symbol and position	1 mark
(ii)	**Faster rise time / faster turn on / less time dissipating power.** (or equivalent)	1 mark

<div align="right"><u>Total for Q6   7</u></div>

7. *(a)* Disc **A   Grey code**

	Disc **B Binary code**	1 mark
(b)	Speed measurement (or equivalent)	1 mark
(c) (i)	**Erroneous position signal when crossing a boundary** (or equivalent)	1 mark
(ii)	**Example such a moving from 000 to 111 can produce 011** (or equivalent)	1 mark
(iii)	**Only one 'bit' changes at a time** (or equivalent)	1 mark

<div align="right"><u>Total for Q7   5</u></div>

8. *(a)* (i) **Provides greater bandwidth for equal voltage gain**   (or equivalent)   1 mark

(ii) **Capacitors block any DC component in the signal**

(or equivalent eg decoupling)	1 mark

(b) (i)

X = **+0.7**V	1 mark
Y = **-0.7**V	1 mark
Z = **0**V	1 mark

(No e.c.f. from X / Y to Z but allow ecf from Z to (ii))

(ii)
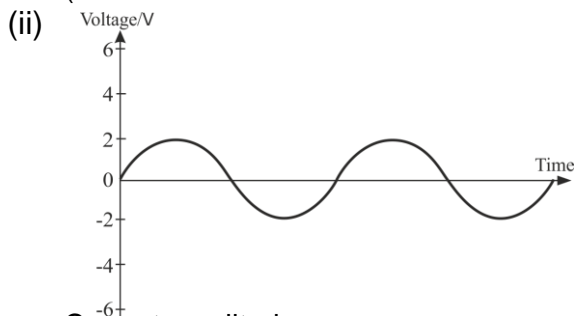
Correct amplitude		1 mark
Correct quiescent voltage	(allow ecf from Z, but ignore phase error	1 mark
(c)	**R_Q >> R_P**	(or equivalent)	1 mark

<div align="right"><u>Total for Q8   8</u></div>