GCE MARKING SCHEME

SUMMER 2019

ELECTRONICS - ET1 (LEGACY)
1141/01

INTRODUCTION

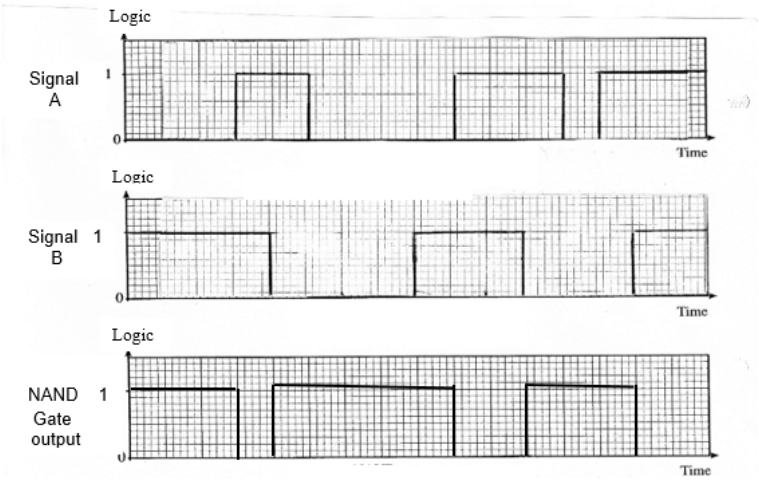
This marking scheme was used by WJEC for the 2019 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

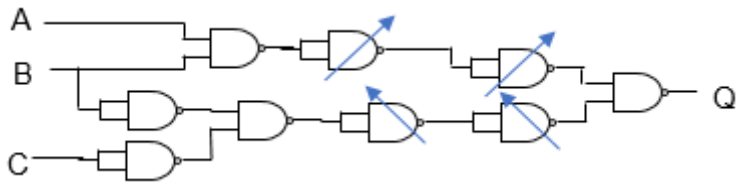
WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

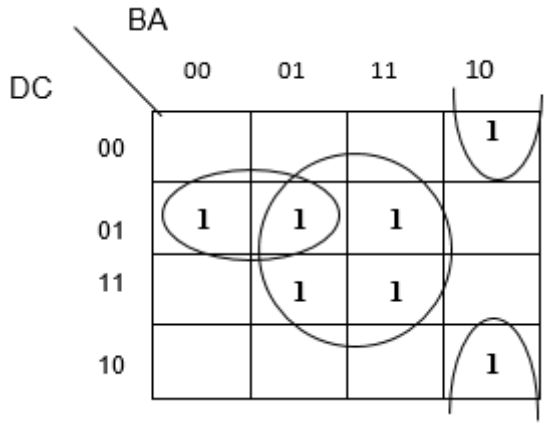
GCE ELECTRONICS - ET1

SUMMER 2019 MARK SCHEME

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>1.</td><td>(a)</td><td></td><td>EXOR gate (1)</td><td>1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>
<table>
<tr><th>B</th><th>A</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
Column Q correct (1)</td><td>1</td></tr>
<tr><td></td><td>(c)</td><td></td><td> 

All 5 transitions correct (1)
Correct logic levels (1)</td><td>1
1</td></tr>
<tr><td></td><td></td><td></td><td>Total for Question 1</td><td>4</td></tr>
</table>

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>2.</td><td>(a)</td><td></td><td>S = B.A (1)
T = $\overline{C+B}$ or $\overline{C}.\overline{B}$ (1)
Q = B.A + $\overline{C+B}$ or B.A + $\overline{C}.\overline{B}$ (1)</td><td>1
1
1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>
<table>
<tr><th>C</th><th>B</th><th>A</th><th>S</th><th>T</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>
Each column S, T and Q correct 1 mark each</td><td>3</td></tr>
<tr><td></td><td>(c)</td><td></td><td> 
</td><td></td></tr>
<tr><td></td><td></td><td>(i)</td><td>Correct NAND replacement of AND gate (1)
Correct NAND replacement of NOR gate (1)
Correct NAND replacement of OR gate (1)</td><td>3</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Two pairs of redundant gates identified (2)</td><td>2</td></tr>
<tr><td></td><td></td><td></td><td>Total for Question 2</td><td>11</td></tr>
</table>

Question			Marking detail	Marks available
3.	*(a)*		$= \overline{X}$	1
	(b)		 Correct map (1) Two groups of 2 and one of 4 identified (ecf map) (1) Any correct term from groups identified (1) Simplest overall expression (1) $Q = C.A + \overline{D}.C.\overline{B}. + \overline{C}.B.\overline{A}$	4
	(c)		$Q = \overline{A}.\overline{\overline{B}.\overline{A}}$ (application of DeMorgan's theorem) (1) $= \overline{A}.B.\ \overline{A}.$ (2 simplifications) (2) $= \overline{A}.B.$ or $Q = \overline{\overline{A + A + \overline{B}}}$ (application of DeMorgan's theorem) (1) $= \overline{A + \overline{B}}$ (simplification) (1) $= \overline{A}.B$ (application of DeMorgan's theorem) (1)	3
			Total for Question 3	**8**

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>4.</td><td>(a)</td><td></td><td>$\overline{Q}$ connected to D x3 (1)
then
Q to clock input on the next IC x2 (1)
with outputs A,B and C to correct Q's (1)

OR
$\overline{Q}$ to clock input on the next IC x2 (1)
with $\overline{Q}$ to outputs A, B and C (1)</td><td>1

1
1</td></tr>
<tr><td></td><td>(b)</td><td></td><td><table><tr><th></th><th>OUTPUT C</th><th>OUTPUT B</th><th>OUTPUT A</th></tr><tr><td>Initial State</td><td>1</td><td>1</td><td>1</td></tr><tr><td>After ONE clock pulse</td><td>1</td><td>1</td><td>0</td></tr><tr><td>After FIVE clock pulses</td><td>0</td><td>1</td><td>0</td></tr></table>One clock pulse outputs correct (1)
Five clock pulse outputs correct (1)</td><td>

1
1</td></tr>
<tr><td></td><td></td><td></td><td>Total for Question 4</td><td>5</td></tr>
</table>

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>5.</td><td>(a)</td><td></td><td>Resistor and switch across power rails and centre connected to input of AND gate (1)
Correct orientation of components (switch top) (1)
Pulse generator connected to the other AND gate input (1)</td><td>1
1
1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>$\overline{Q}$ = 1 (1)</td><td>1</td></tr>
<tr><td></td><td>(c)</td><td></td><td>High enough frequency to make it random/unpredictable/ impossible to cheat (owtte) (1)</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td>Total for Question 5</td><td>5</td></tr>
<tr><td>6.</td><td>(a)</td><td>(i)</td><td>
<table>
<tr><th>C</th><th>B</th><th>A</th><th>RED</th><th>BLUE</th><th>GREEN</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
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<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table>
Columns RED and BLUE correct 1 mark each</td><td>2</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>NAND gate (1)
Inputs connected to A and C (1)</td><td>1
1</td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>40 (1)</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>10 ecf from (i) (1)</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td>Total for Question 6</td><td>6</td></tr>
</table>

Question			Marking detail	Marks available
7.	(a)	(i)	Voltage gain = -120/10 = -12 (1)	1
		(ii)	Output voltage = -12x0.8 = -9.6 (1) ecf on -12 additional mark for BOTH minus signs in (i) and (ii) (1)	1 1
		(iii)	bandwidth = $2.4 10^6$/12 (1) ecf on -12 = 200k(Hz) or 0.2M(Hz) or 200000 (Hz) (1)	1 1
	(b)	(i)	R = 240 kΩ (1)	1
		(ii)	Output voltage saturated / (-)15V (1)	1
	(c)	(i)	No change (in input impedance) (1)	1
		(ii)	bandwidth has REDUCED / HALVED / = 100k(Hz) (1)	1
	(d)		Rearrange formula $\Delta t = \Delta V_{OUT}$/slew-rate and substitution = 24/5 (1) =4.8 (1) Correct unit **us** (1)	1 1 1
			Total for Question 7	**12**
8.	*(a)*	(i)	V_{IN} connected directly to non-inverting input (1) Feedback resistor between output and inverting input (1) Resistor between inverting input and 0V rail (1)	1 1 1
		(ii)	Resistor ratio 39:1 and both 1kΩ or greater (1) Resistors labelled on diagram correctly or unambiguously identified. (1)	1 1
	(b)		Non-inverted saw-tooth wave drawn (1) Correct time scale (1) Peaks at ±8V on first cycle (1) Saturates at ±11V on second cycle (1)	1 1 1 1
			Total for Question 8	**9**