Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A Level – LEGACY

1141/01

S19-1141-01

ELECTRONICS – ET1

MONDAY, 13 MAY 2019 – MORNING

1 hour 15 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**4**	
2.	**11**	
3.	**8**	
4.	**5**	
5.	**5**	
6.	**6**	
7.	**12**	
8.	**9**	
Total	**60**	

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ADDITIONAL MATERIALS

A calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B+1) = A$$

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Answer **all** *questions.*

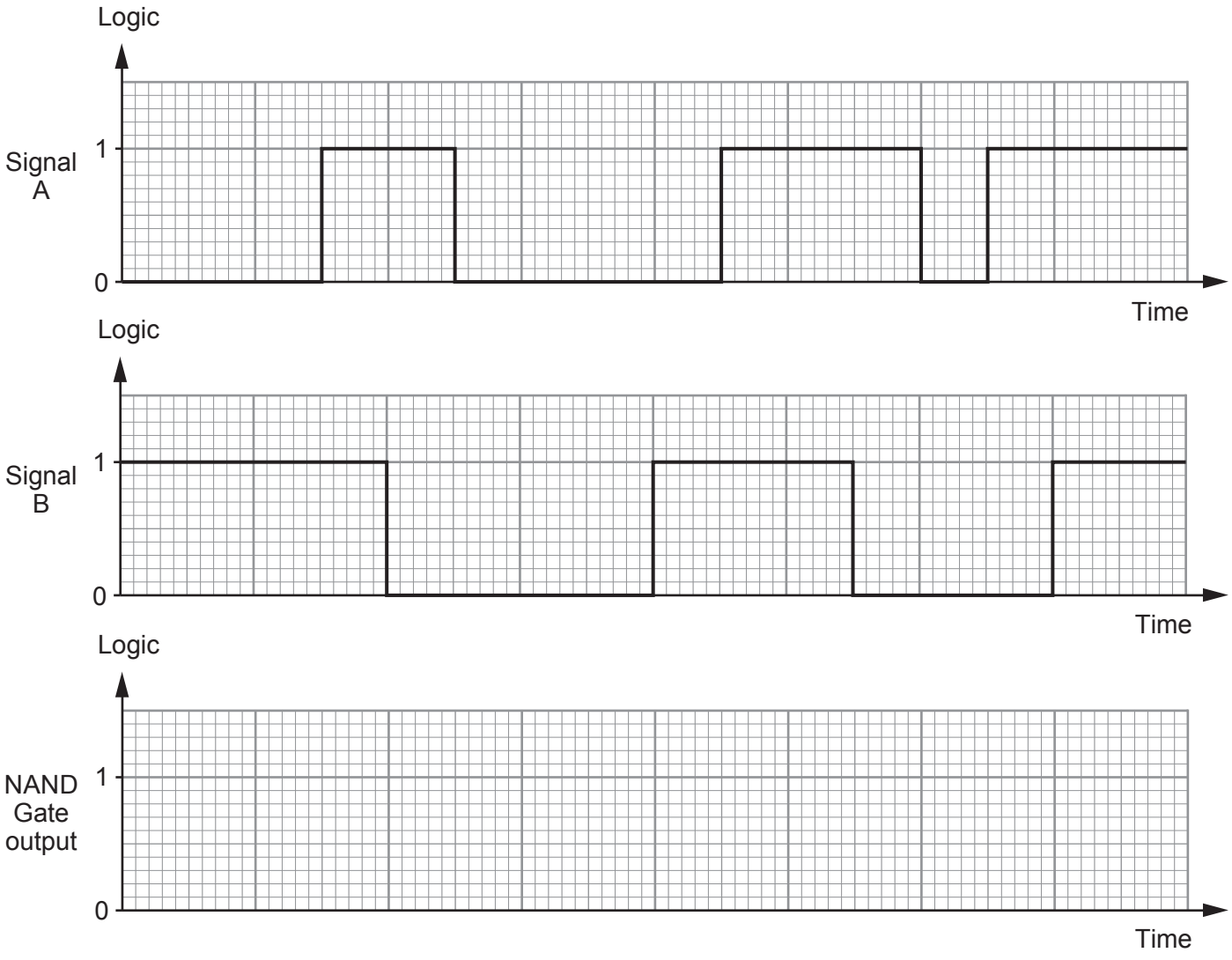
1. *(a)* Which 2-input logic gate outputs a logic 1 only when both inputs are different? [1]

.....

(b) Complete the truth table for a 2-input NAND gate. [1]

B	A	Q
0	0	
0	1	
1	0	
1	1	

(c) Signals A and B are applied to the inputs of a 2-input NAND gate. Sketch the output. [2]



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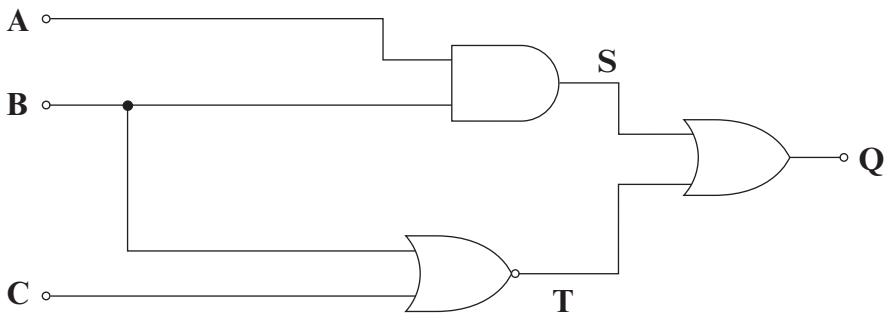
2. The diagram shows a logic system.



(a) Write down the Boolean expression for each of the outputs **S**, **T** and **Q** in terms of inputs **A**, **B** and **C**. [3]

S = ...

T = ...

Q = ...

(b) Complete the truth table for this system. [3]

C	B	A	S	T	Q
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

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(c) (i) In the space below, draw the same logic system, but with the logic gates replaced by their NAND equivalents. [3]

(ii) Cross out all redundant gates. [2]

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Turn over.

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3. *(a)* Simplify the following expression.

$\overline{X} + \overline{X}.Y =$ ..... [1]

(b) Using a Karnaugh map or Boolean algebra, simplify the following expression as much as possible. [4]

$$Q = C.B.A + \overline{D}.\overline{C}.B.\overline{A} + \overline{D}.C.\overline{B}.\overline{A} + C.\overline{B}.A + D.\overline{C}.B.\overline{A}$$

.....

.....

.....

.....

.....

DC \ BA	00	01	11	10
00				
01				
11				
10				

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. [3]

$$Q = \overline{\overline{A} + \overline{B}.\overline{\overline{A}}}$$

.....

.....

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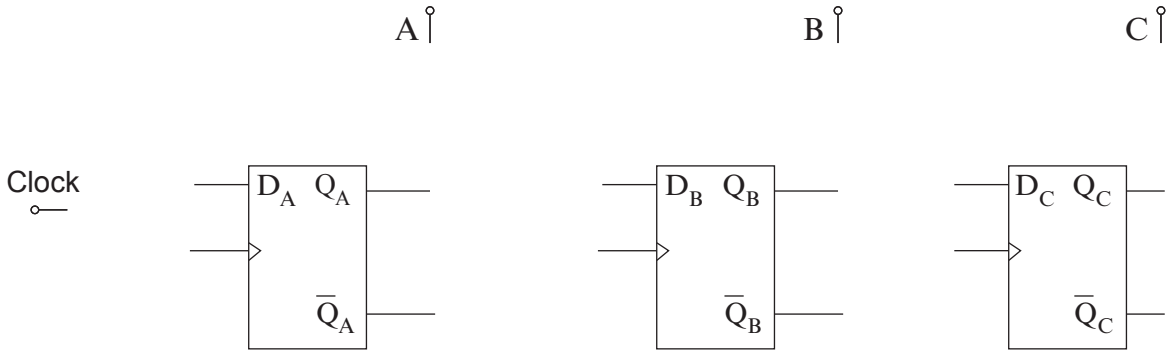
4. The diagram shows three D-type flip-flops, which form part of a binary **down-counter**. Outputs A, B and C are used to indicate the binary output. A is the **least significant** bit.



(a) Complete the diagram to make a three-bit binary **down-counter**. [3]

(b) The initial state of the counter is shown in the table. Complete the table, using 0 or 1, to indicate the logic state of each output after the stated number of clock pulses. [2]

	OUTPUT C	**OUTPUT B**	**OUTPUT A**
Initial State	1	1	1
After ONE clock pulse			
After FIVE clock pulses			

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Turn over.

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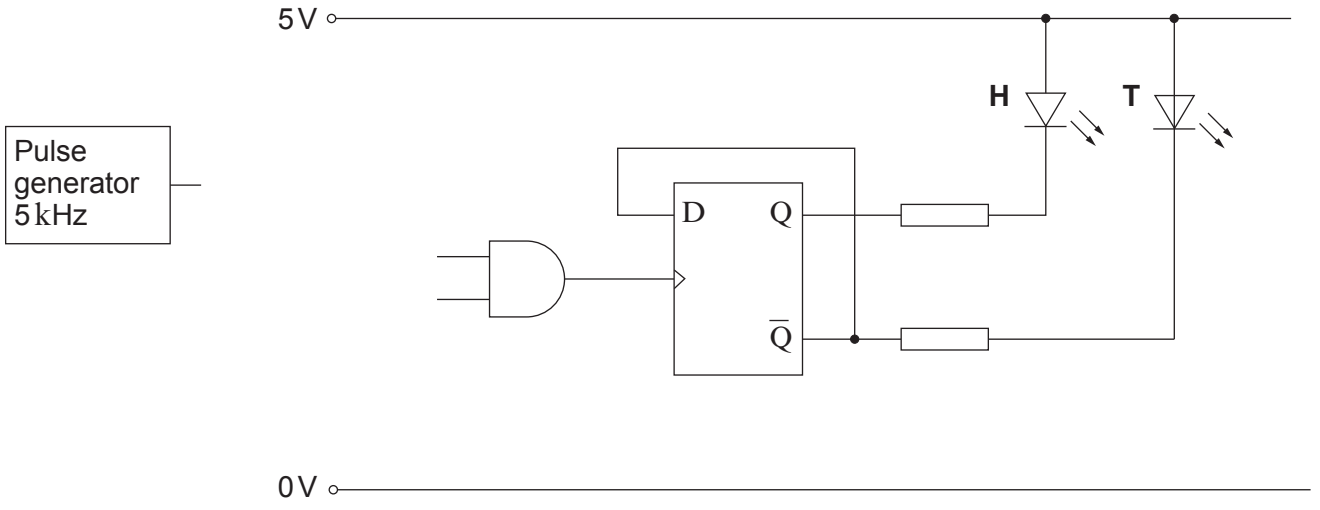
5. The diagram shows an incomplete circuit for an electronic coin-tossing game in which **LED H** represents heads and **LED T** represents tails. A switch is pressed to start the LED's flashing. When the switch is released either **H** or **T** stays lit.



(a) Add the necessary components and connections to the diagram to complete the circuit so that it meets the specification. [3]

(b) What is the logic state of $\overline{Q}$ when **LED T** is off? [1]

Logic state of $\overline{Q}$ = ...

(c) Why is a frequency of 5 kHz suitable for this application? [1]

.....

.....

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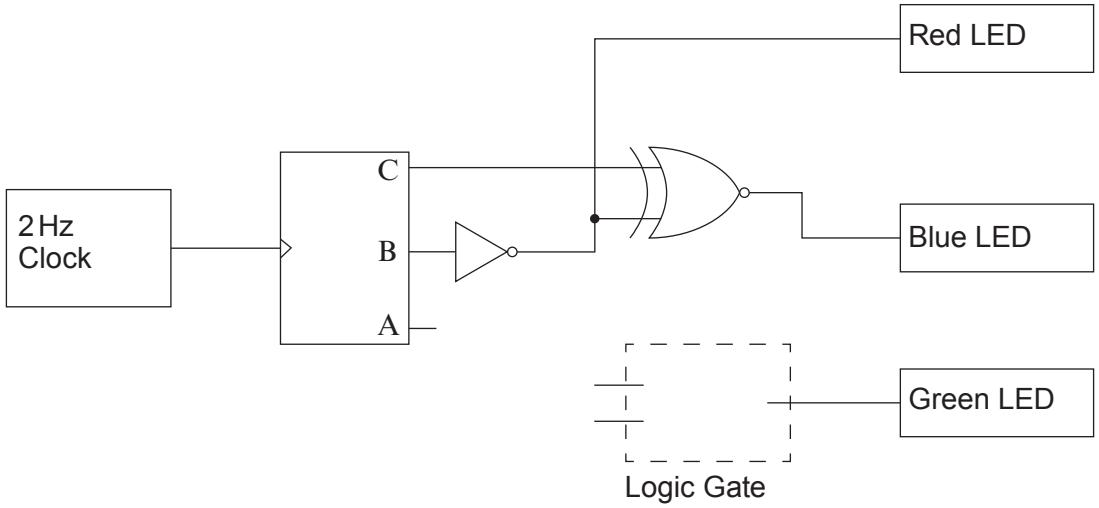
6. The diagram shows the control system for a LED display that uses a 3-bit counter. A LED is on when a logic 1 is applied to the input. All the LEDs are initially off.



(a) (i) Complete the truth table for columns red and blue. [2]

C	B	A	Red	Blue	Green
0	0	0			1
0	0	1			1
0	1	0			1
0	1	1			1
1	0	0			1
1	0	1			0
1	1	0			1
1	1	1			0

(ii) In the dotted box above draw the 2-input logic gate that will produce the green output and include the connections to the counter. [2]

(b) (i) How many pulses does the 2 Hz clock produce in 20 seconds? [1]

.....

(ii) How many times does the red LED flash in 20 seconds? [1]

.....

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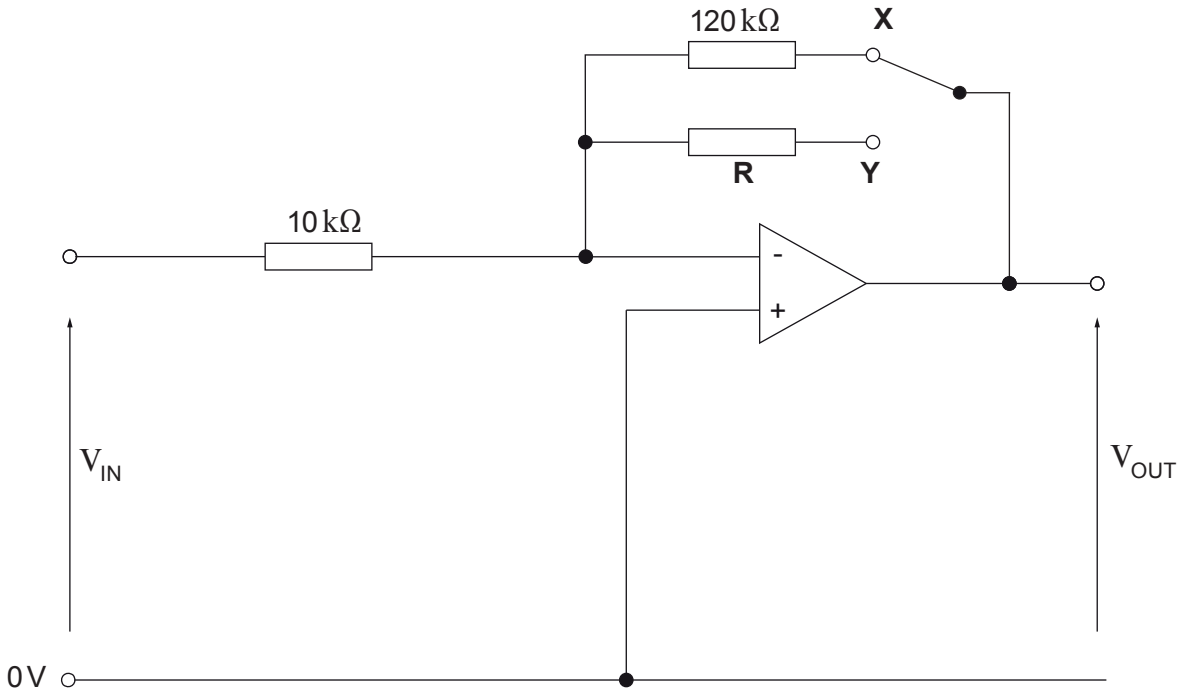
7. An extract from the data sheet of an op-amp is shown in the following table.

Parameter	Value
Input Impedance	$10\,\mathrm{M\Omega}$
Output Impedance	$100\,\Omega$
Open Loop Gain	10^5
Gain Bandwidth Product	$2.4\,\mathrm{MHz}$
Slew Rate	$5\,\mathrm{V\mu s^{-1}}$

The circuit diagram shows the op-amp set up as a voltage amplifier. The switch allows the user to change the gain.



An input voltage of 0.8 V is applied to V_{IN}.

The op-amp is powered from a ± 16 V supply and saturation occurs at ± 15 V.

(a) The switch is initially connected to point **X**. [5]

(i) Calculate the voltage gain of the amplifier.

.....

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(ii) Calculate the output voltage when V_{IN} = 0.8 V.

.....

.....

.....

(iii) Calculate the bandwidth of the amplifier.

.....

.....

.....

(b) The switch is moved from **X** to **Y**. This **doubles** the voltage gain of the amplifier. [2]

(i) Calculate the value of resistor **R**.

.....

.....

(ii) Determine the output voltage for V_{IN} = 0.8 V.

.....

.....

(c) State what change, **if any**, occurs to the following when the switch is moved from **X** to **Y**. [2]

(i) The input impedance .....

(ii) The bandwidth .....

(d) Calculate the time it would take for the output voltage to change from –12 V to +12 V in response to a large step change in input voltage.
Show your working and give the appropriate unit. [3]

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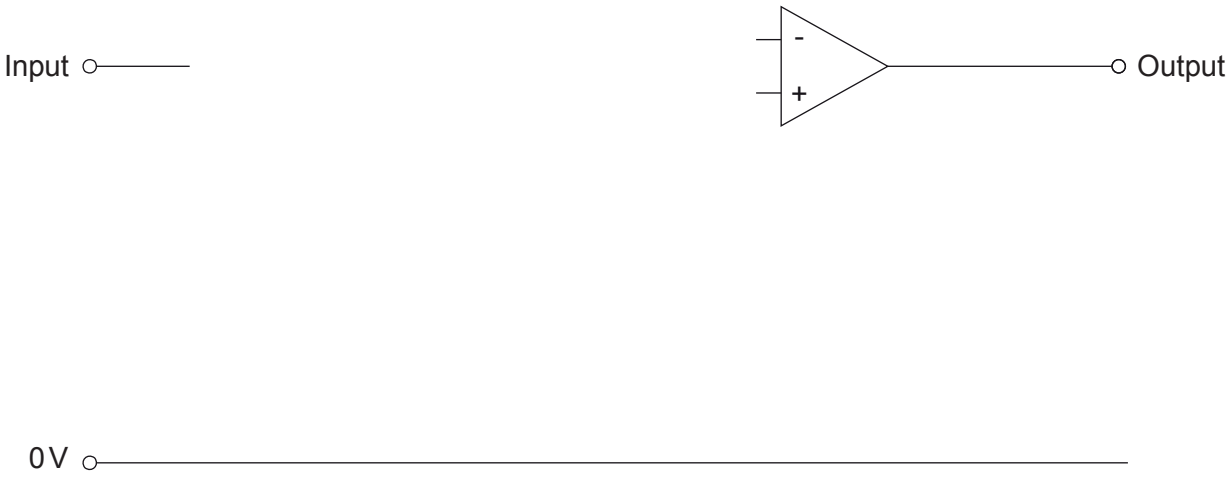
8. *(a)* (i) Complete the circuit diagram for a non-inverting amplifier. [3]



(ii) Calculate component values to give a voltage gain of 40. Label the diagram with these values. [2]

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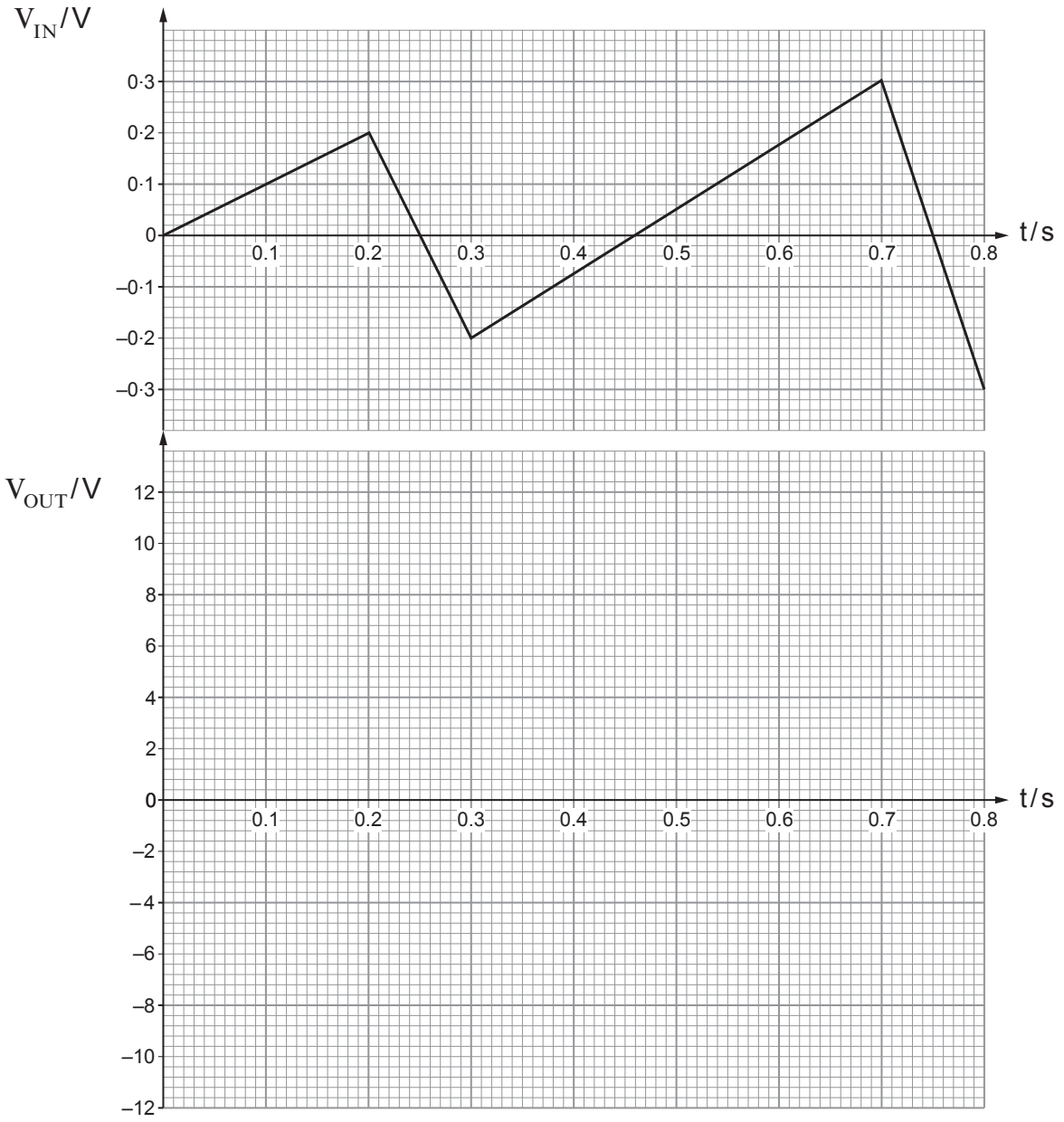
(b) The upper graph shows a signal applied to the input of the voltage amplifier. Draw the output voltage on the axes provided. The op-amp is powered from a ± 12 V supply and saturation occurs at ± 11 V. [4]



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