GCE MARKING SCHEME

SUMMER 2019

ELECTRONICS - ET2 (LEGACY)
1142-01

INTRODUCTION

This marking scheme was used by WJEC for the 2019 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

GCE ELECTRONICS - ET2

SUMMER 2019 MARK SCHEME

Question			Answers/Explanatory Notes *Indicates that ECF will be allowed from a previous part of the question	Marks Available
1.	(a)		V_1 =6 V (1)	7
	(b)		R_1 = 2 k Ω (1) *	
	(c)		I_1 =5 mA (1) *	
	(d)		I_2 =2 mA (1) *	
	(e)		R_2 = 3 k Ω (1) *	
	(f)		R_{EFF} = 1.2 k Ω (1) * Correct use of Ohm's law in part b or c above (1)	**[7]**
2.	(a)	(i) (ii) (iii)	V_{OC} = 7.2 V (1) I_{SC} = 1 A (1) R_O = 7.2 Ω (1) *	3
	(b)	(i)	Correct equivalent circuit (1) *	3
		(ii)	Voltage drop across R_O = 0.9 V (1) * Maximum load current = 0.9V/ 7.2 = 0.125 A (1) * [Accept any other method that makes use of equiv cct]	**[6]**
3.	(a)		Switching threshold at 2 and 4 units on time axis 2 x (1) Inverted o/p and amplitude = 10 V (1)	3
	(b)	(i)	Resistor and LDR in voltage divider (1) Correct orientation (1) One resistor is variable (1) LED and resistor in series between op-amp o/p and 0/9 V depending on orientation of sensing circuit (1) *	4
		(ii)	V_{IN} = 4.5 V (1)	1
				[8]

Question			Answers/Explanatory Notes *Indicates that ECF will be allowed from a previous part of the question	Marks Available
4.	(a)	(i)	V_{rms} = 8.5 V (1)	2
		(ii)	V_{OUT} =11.3 V (1)	
	(b)		2 positive sinusoidal voltages pulses (1) 11.3 V peak (1) *	2
	(c)	(i)	Capacitor across output (1)	1
		(ii)	Smoothed output /correct shape of graph for HWR (1) Small ripple with peaks at 11.3 V (1) *	2
	(d)	(i)	10.6 V (1)	2
		(ii)	Smaller/halves (1)	
				[9]
5.	(a)		Substitution with correct multipliers (1) 47s (1)	2
	(b)	(i)	T =0.69 RC (1) 32.4s (1) *	2
		(ii)	Substitution (1) 1.92V (1)	2
		(iii)	Approx. 10 V (1) *	1
				[7]
6.	(a)		V_R =15 – 10 = 5 V (1) I_R = 120 +5 = 125mA (1) R = 5 V /125mA = 40 Ω (1) *	3
	(b)	(i)	75mA (1)	3
		(ii)	P = 10 x 75 (1) * = 750mW [0.75W] (1) *	
	(c)		R = 39Ω. 47Ω would not allow a 120mA load current (1) *	1
				[7]
7.	(a)		Correct shape and 2 (accept 3) whole cycles (1) 2: 1 M/S ratio (1)	2
	(b)		Rearranging formula (1) Substitution with correct multipliers (1) R_B =13kΩ (1)	3
	(c)		R_A =13kΩ (1) *	1
				[6]

Question			Answers/Explanatory Notes *Indicates that ECF will be allowed from a previous part of the question	Marks Available
8.	(a)	(i)	I_B = 1200mA/240Ω (1) = 5mA (1)	2
		(ii)	Voltage across 1.1k Ωres = 5 mA x 1.1k Ω = 5.5V (1) * V_{IN} = 5.5 +0.7 = 6.2 V (1) *	2
	(b)		Shape (1) Plotting point (0.7, 15) Allow tolerance of ± 0.1 V (1) * Plotting point (6.2, 0) Allow tolerance of ± 0.1 V (1) *	3
	(c)	(i)	V_{OUT} = 5V (1)	1
		(ii)	Transistor would overheat/significant power dissipated in transistor (1) Voltage across solenoid = 10 V so it would not operate/ not operate correctly (1)	2
				[10]
TOTAL				**60**