GCE MARKING SCHEME

SUMMER 2019

ELECTRONICS - ET5 (LEGACY)
1145/01

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INTRODUCTION

This marking scheme was used by WJEC for the 2019 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

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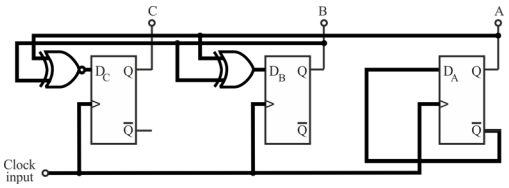
GCE ELECTRONICS - ET5

SUMMER 2019 MARK SCHEME

1. *(a)* (i) Time delay between change at input of system and resulting change at output.
(or equivalent answer.) 1 mark

(ii) All stages receive clock pulses simultaneously, and so all change at the same time when a clock pulse is received. 1 mark

(b) (i)



Correct **clock** connections 1 mark
Use of **EXNOR** gate with correct inputs for D_C or use of NOT gate 1 mark
Use of **EXOR** gate with correct inputs for D_B or use of NOT gate 1 mark
Use of $\overline{\mathbf{Q}}_{\mathbf{A}}$ 1 mark

(ii)

State	C	B	A	D_C	D_B	D_A
0	0	1	0	**0**	**1**	**1**
1	**0**	**1**	**1**	**1**	**0**	**0**
2	**1**	**0**	**0**	**1**	**0**	**1**
3	**1**	**0**	**1**	0	1	0

1 mark per transition x 3 3 marks

(iii)

State	C	B	A		C	B	A
4	**0**	**0**	**0**		**1**	**0**	**1**
5	**0**	**0**	**1**		**0**	**1**	**0**
6	**1**	**1**	**0**		**0**	**1**	**1**
7	**1**	**1**	**1**		**1**	**0**	**0**

1 mark per transition x 4 4 marks

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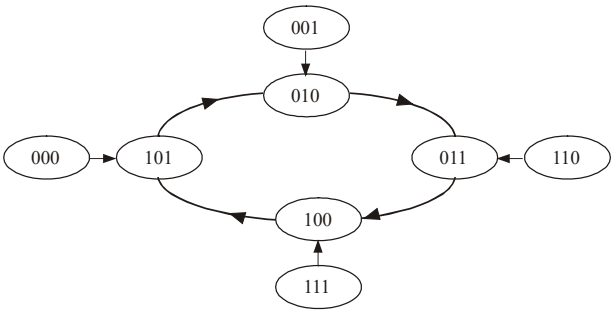
(iv)



Main sequence	1 mark
Unused states	1 mark

Total for Q1 15

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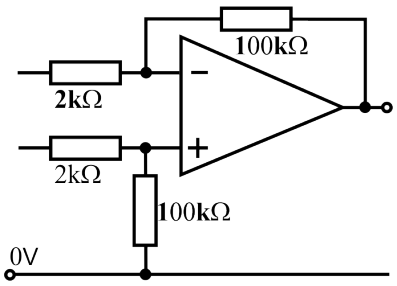
2. *(a)* Use of variable resistor in one limb 1 mark

Any bridge arrangement with T_{IN} and T_{OUT} 1 mark

Correct orientation 1 mark

(b)



(i) Correct connections to inverting input 1 mark

Correct connections to non-inverting input 1 mark

(ii) Resistor ratio = 50:1 1 mark

(c) (i) Voltage at R = 40mV 1 mark

Voltage at Q = 80mV 1 mark

Voltage at P = 120mV 1 mark

(ii)

Output of Diff amplifier	V_W	V_X	V_Y	Binary output	
				B	A
0.03V	0	0	0	0	0
0.10V	12	12	0	1	0

Correct op-amp outputs for 0.03V 1 mark
Correct binary output for 0.03V 1 mark
Correct op-amp outputs for 0.10V 1 mark
Correct binary output for 0.10V 1 mark

(iii) Indicate when input exceeds input voltage range, or equivalent 1 mark

(iv) Resolution is reduced equivalent 1 mark

(v) No. of comparators = 256 1 mark

Total for Q2 16

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3. *(a)* Active filters can have gain >1 (or equivalent) 1 mark

(b) Filter **D** = Treble cut 1 mark

Filter **B** = Bass boost 1 mark

(c) Reactance = 24kΩ at the break frequency (= 200Hz), or equivalent 1 mark

(d) (i) Amplitude at output of A = **200mV** 1 mark

(ii) Frequency at output of A = **500Hz** 1 mark

(e) (i) Resistor 1 = **200kΩ** 1 mark

Resistor 2 = **10kΩ** 1 mark

(ii) Capacitor = **1nF** 1 mark

Use of 200kΩ resistor in break frequency formula (allow ecf)1 mark

Total for Q3 10

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4. *(a)* If monitoring the stop button were part of the main program, the response would be delayed if the main program were executing one of the delay subroutines when the stop button was pressed. or equivalent answer 1 mark

(b)
```
movlw   b'10010000'

movwf   INTCON
```

Global interrupt AND Port B0 interrupt enabled 1 mark
All other bits correct 1 mark

(c) (i) Instruction protects the contents of the working register as it enters the ISR so that they can be recovered when the program returns to the main program on completing the ISR.
or equivalent answer 1 mark

(ii)
```
movf    tempstore
```
1 mark

(d)
```
repeat  bsf     PORTA,0
        bcf     PORTA,1
        call    onesec
        bsf     PORTA,1
        bcf     PORTA,0
        call    onesec
```

Correct control of lamp X 1 mark
Correct control of lamp Y 1 mark
Correct timing 1 mark

(e)
```
btfss   PORTB,2
goto    repeat
```
1 mark
1 mark

Total for Q4 10

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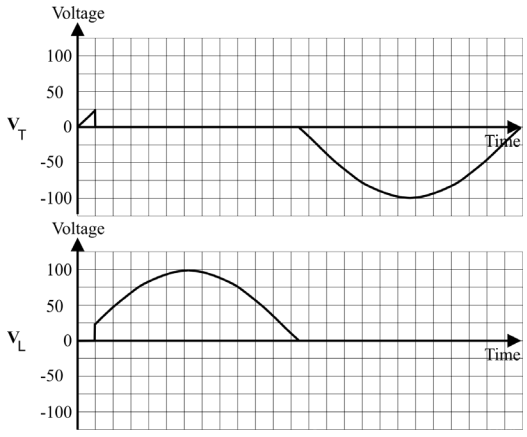
5.	*(a)*	(i)	Best input impedance = 1600kΩ	1 mark
		(ii)	Best output impedance = 16Ω	1 mark
	(b)	(i)	Overall gain = product of gains = 625	1 mark
		(ii)	Bandwidth = 240kHz (allow ecf from (i))	1 mark
			Use of gain-bandwidth product	1 mark
	(c)	(i)	Voltage at P = 6.0V	1 mark
		(ii)	Output voltage = 5.3V (allow ecf from (i))	1 mark
		(iii)	Voltage across transistor = 6.7V (allow ecf from (ii))	1 mark
		(iv)	Power dissipation = 1.3W (allow ecf from (iii))	1 mark
		(v)	Max. power dissipated in speaker = 1.125W	1 mark
			Use of 12V in max. power formula	1 mark

Total for Q5 11

6.	*(a)*	Thyristor added correctly	1 mark
		Diac added correctly	1 mark
	(b)	Phase angle = **72.3^0**	1 mark
		Use of X_C	1 mark
		Re-arranged formula	1 mark



(c)	Switching at 25V	1 mark
	V_T correct	1 mark
	V_L correct	1 mark

Total for Q6 8

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