Surname	Centre Number	Candidate Number
Other Names		2

GCE AS – NEW

B490U10-1

S19-B490U10-1

ELECTRONICS – AS component 1
Principles of Electronics

MONDAY, 13 MAY 2019 – MORNING

2 hours 30 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**9**	
2.	**10**	
3.	**10**	
4.	**9**	
5.	**7**	
6.	**11**	
7.	**9**	
8.	**14**	
9.	**10**	
10.	**16**	
11.	**15**	
Total	**120**	

B490U101
01

ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Answer **all** questions.

Write your name, centre number and candidate number in the spaces at the top of this page.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in questions **8***(b)* and **11***(c)*.

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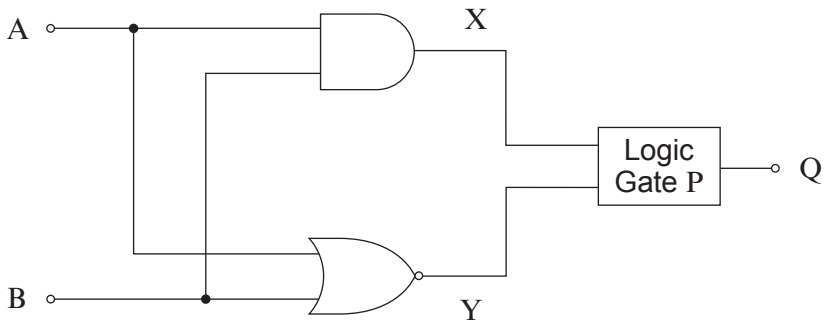
Answer **all** *questions.*

1. *(a)* Complete the truth table for a two-input EXNOR gate. [1]

B	A	Q
0	0	
0	1	
1	0	
1	1	

(b) An EXNOR gate can be built from other logic gates. Complete the truth table for X, Y and Q and hence identify logic gate 'P' so that the circuit produces the same output as an EXNOR gate. [3]



B	A	X	Y	Q
0	0			
0	1			
1	0			
1	1			

Logic gate P .....

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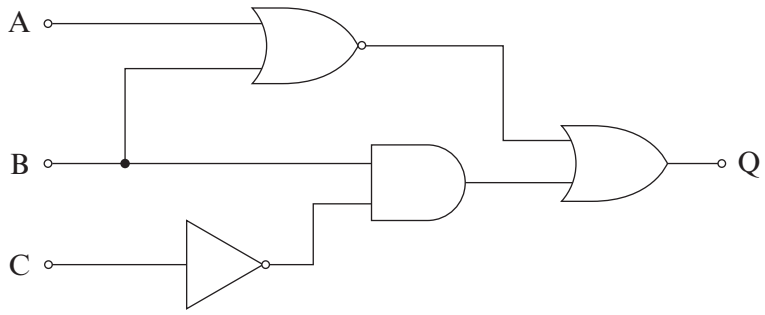
(c) The following diagram shows another logic system.



In the space below, draw the equivalent logic system to the one shown, but with the logic gates replaced by NAND gates. Cross out all redundant gates. [5]

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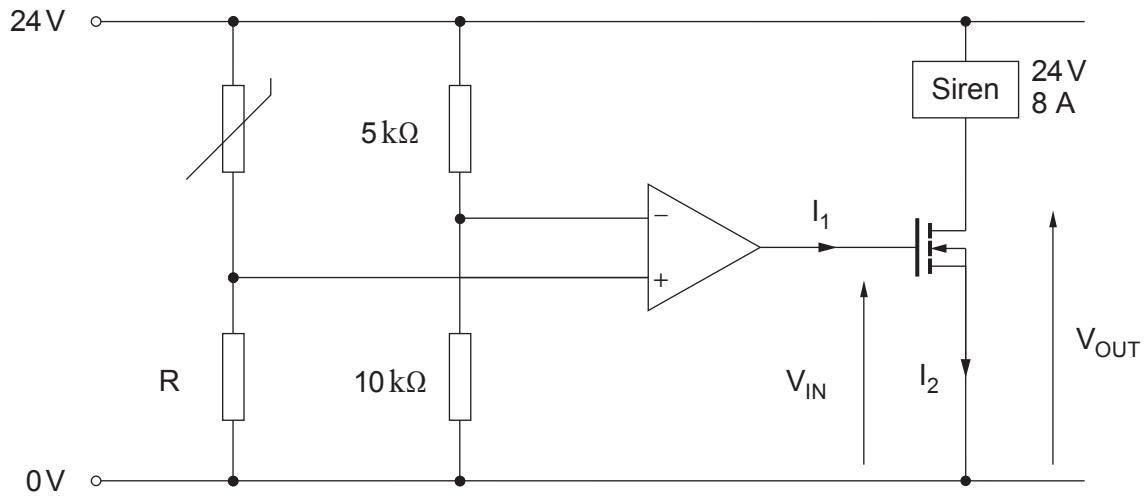
2. A large walk-in refrigerator has an electronic alarm system designed to sound a high-powered siren if the temperature goes above 4°C.



The thermistor has a resistance of 3.2 kΩ at 4 °C.

(a) Determine a suitable value for R. [2]

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(b) Explain how to adapt the circuit to allow adjustment of the temperature at which the alarm is triggered. [1]

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(c) An engineer tests the system and records the following parameters when the MOSFET just saturates.

V_{IN} / V	V_{OUT} / V	I_2 / A
6.5	1.38	7.94

(i) Estimate the value of I_1. ..... [1]

(ii) Use the results to calculate:

(I) the value of g_M. [3]

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(II) the value of r_{DSon}. [3]

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3. *(a)* Simplify the following expressions showing working where appropriate.

(i) $\overline{A}.1$ = ... [1]

(ii) $(B + \overline{A}).(\overline{B} + A)$ = ...

..... [2]

(b) Using a Karnaugh map simplify the following expression as much as possible. [4]

$$Q = D.C.A + \overline{D}.C.B.A + \overline{C}.\overline{B}.\overline{A} + C.\overline{B}.A + D.C.B$$

DC \ BA	00	01	11	10
00				
01				
11				
10				

Q = ...

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. All steps of the simplification must be shown. [3]

$$Q = \overline{(\overline{A}.\overline{B}).(A + \overline{B})}$$

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4. A simple clock requires an astable sub-system to produce a 1 Hz signal.

(a) Design a 1 Hz astable circuit based upon a Schmitt inverter. Your design should include a circuit diagram with all component values clearly labelled. A 6.8 μF capacitor is used in the circuit. [4]

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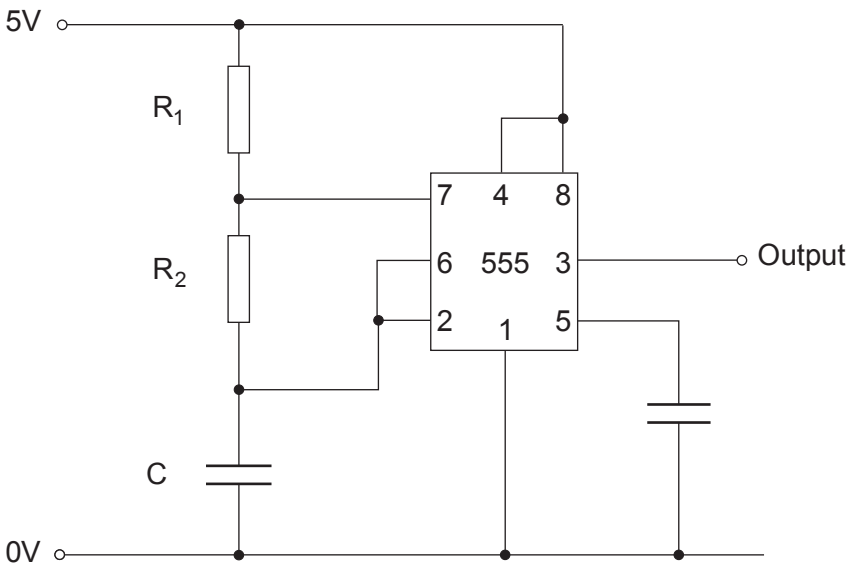
(b) An alternative solution is based on a 555 timer astable circuit as shown below.



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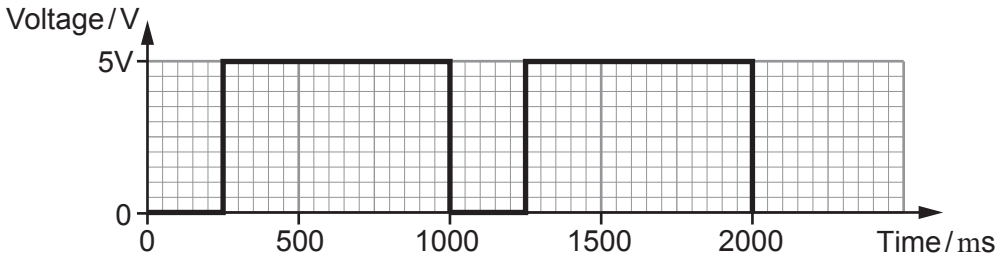
The following graph shows the output signal for two cycles.



(i) Determine the mark:space ratio for this signal. [1]

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(ii) Capacitor C has a value of 22 μF. Calculate the value of resistor R_2 that will produce a space duration of 250 ms. [3]

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(c) Determine the value of resistor R_1. [1]

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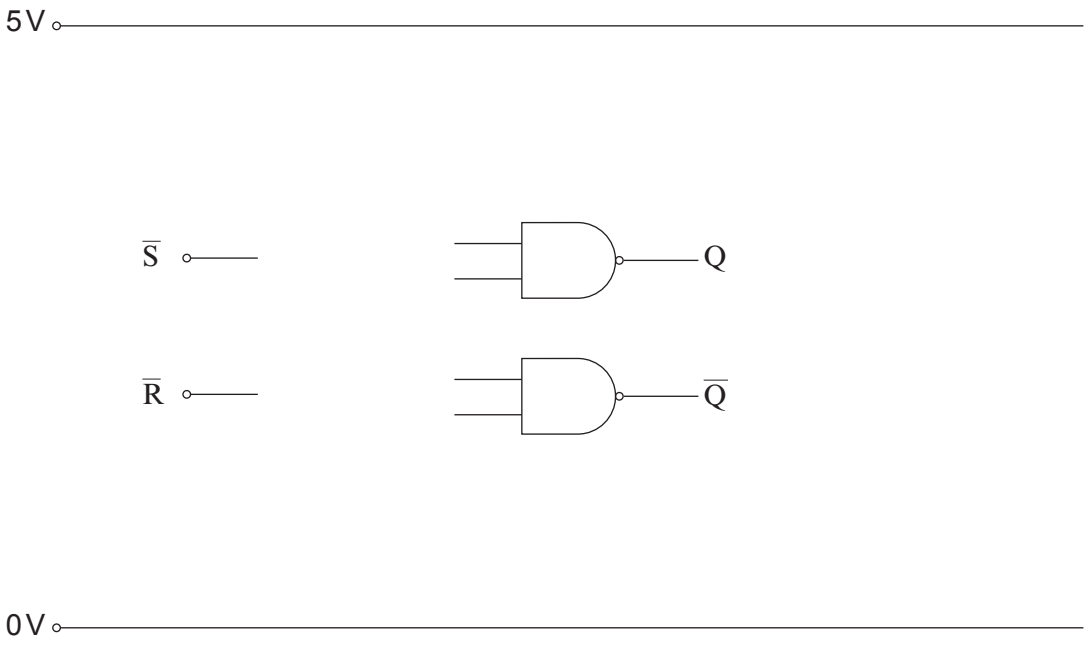
5. *(a)* Complete the diagram to show how two NAND gates can be connected to make a $\overline{S}.\overline{R}$ bistable (latch). Add the appropriate components so that an LED connected to Q is **on** when Q is **low**. [3]



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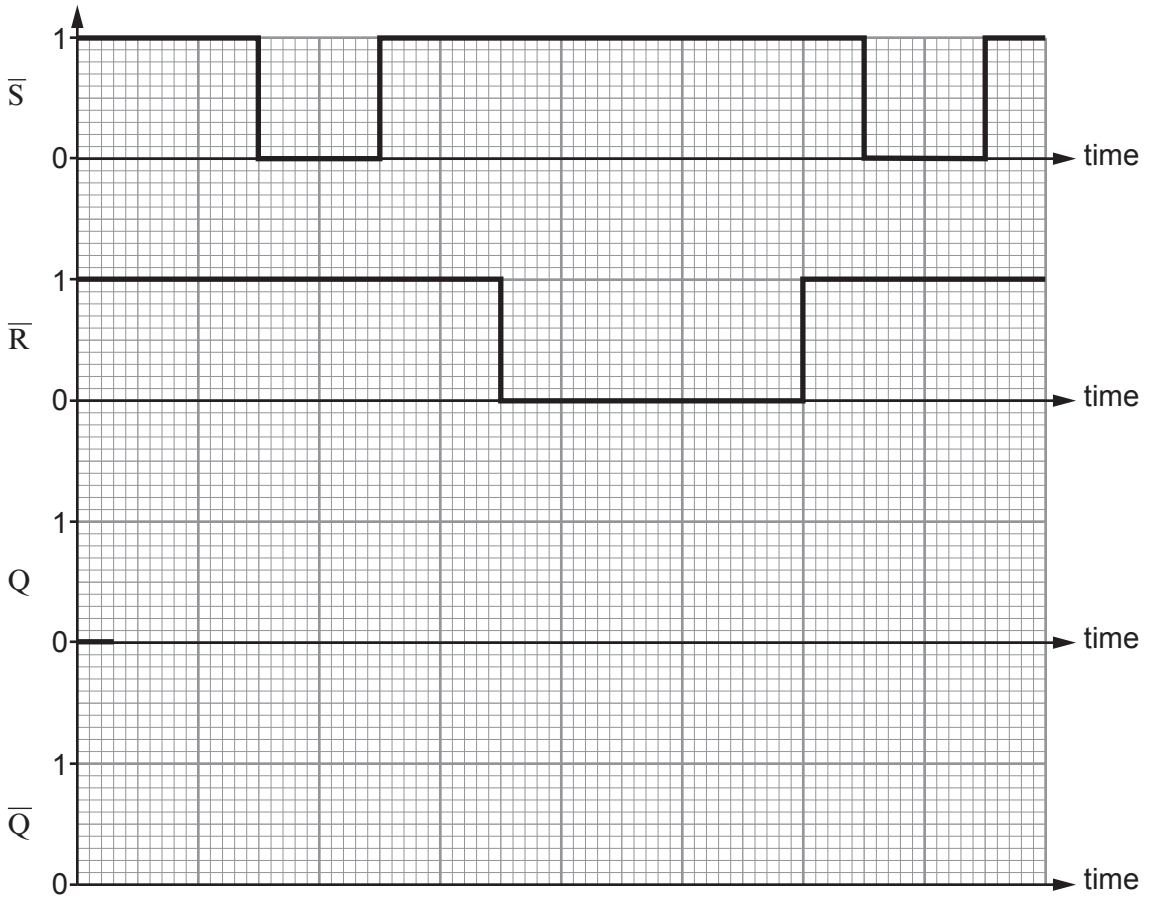
(b) Pulses are applied to the two inputs as shown below. Draw the corresponding output pulses at Q and $\overline{Q}$ on the axes provided. **Q is initially at logic 0**. [3]



(c) Why is it desirable that $\overline{S}$ and $\overline{R}$ are prevented from being logic 0 at the same time? [1]

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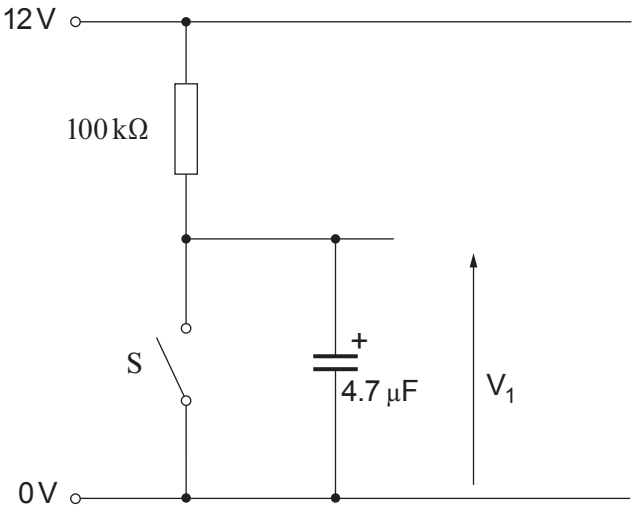
6. *(a)* The diagram shows a timing sub-system.



(i) Switch S is closed then released at time t = 0. Determine the time taken for V_1 to reach 6 V. [3]

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(ii) Calculate the value of V_1 at a time of t = 1 s. [3]

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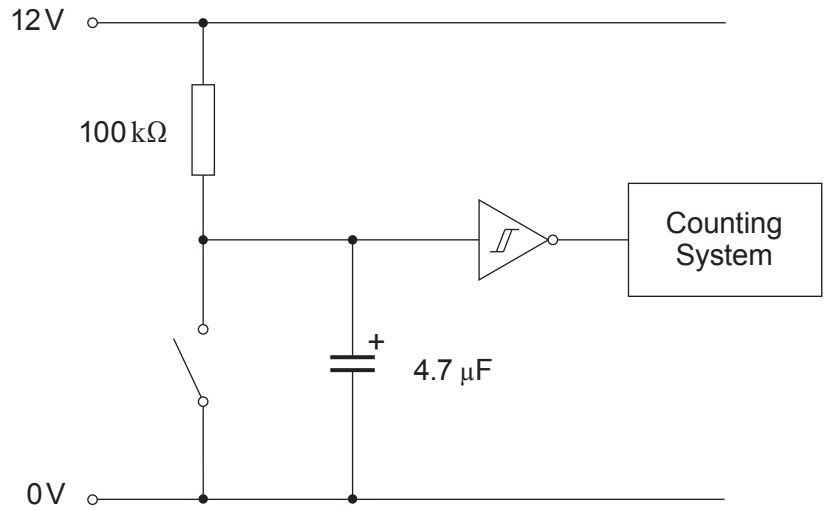
(b) A small theatre in a theme park shows a virtual reality presentation every 15 minutes. The following circuit is used in the turnstile. It incorporates the timing sub-system from part *(a)* in a counting circuit.



What is the combined effect of the timing sub-system and the Schmitt inverter on the signal from the switch and why is it needed in this system? [2]

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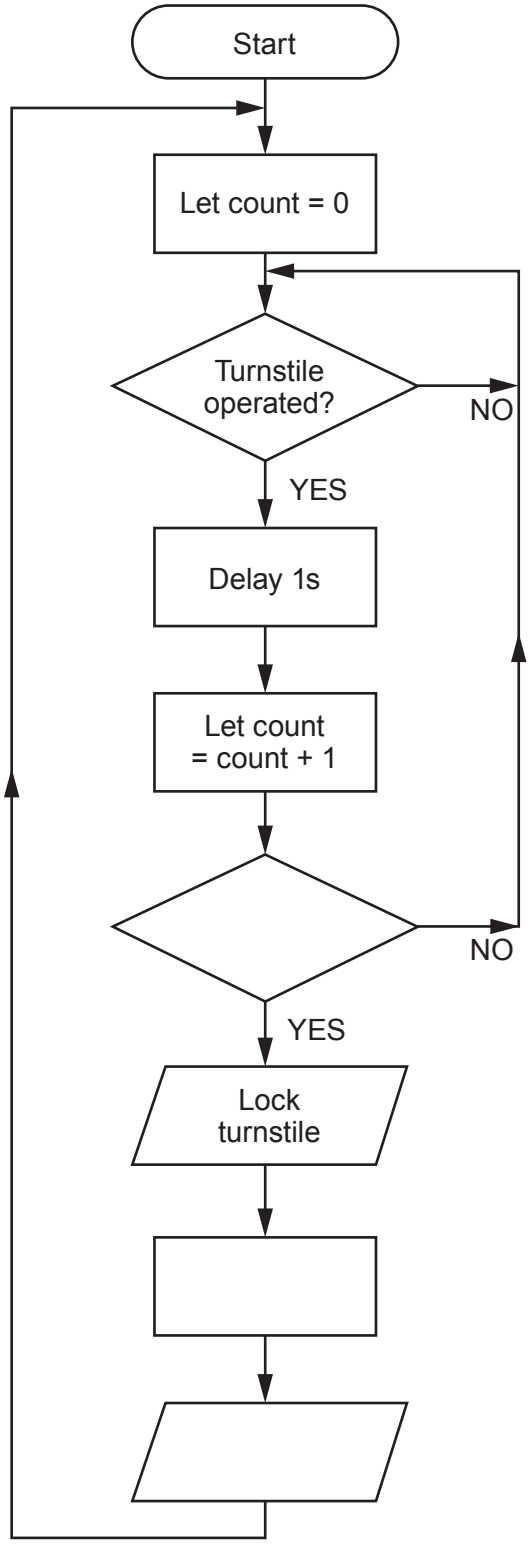
(c) An alternative design for the theatre entry system is controlled by a microcontroller that must satisfy the following specification.

- Only 50 people are allowed to enter through the turnstile
- Once 50 people have entered, the turnstile will lock for 15 minutes
- After 15 minutes the system will reset ready for the next presentation

Complete the design for a flowchart for the theatre entry program. [3]



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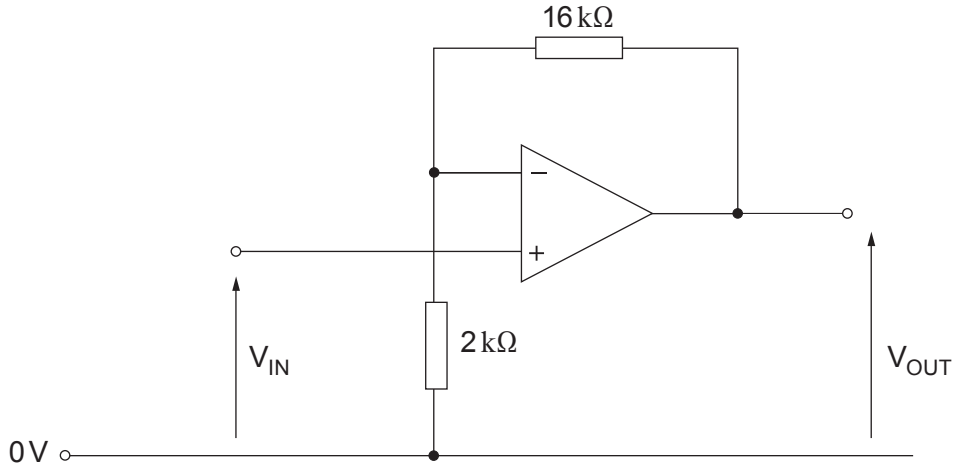
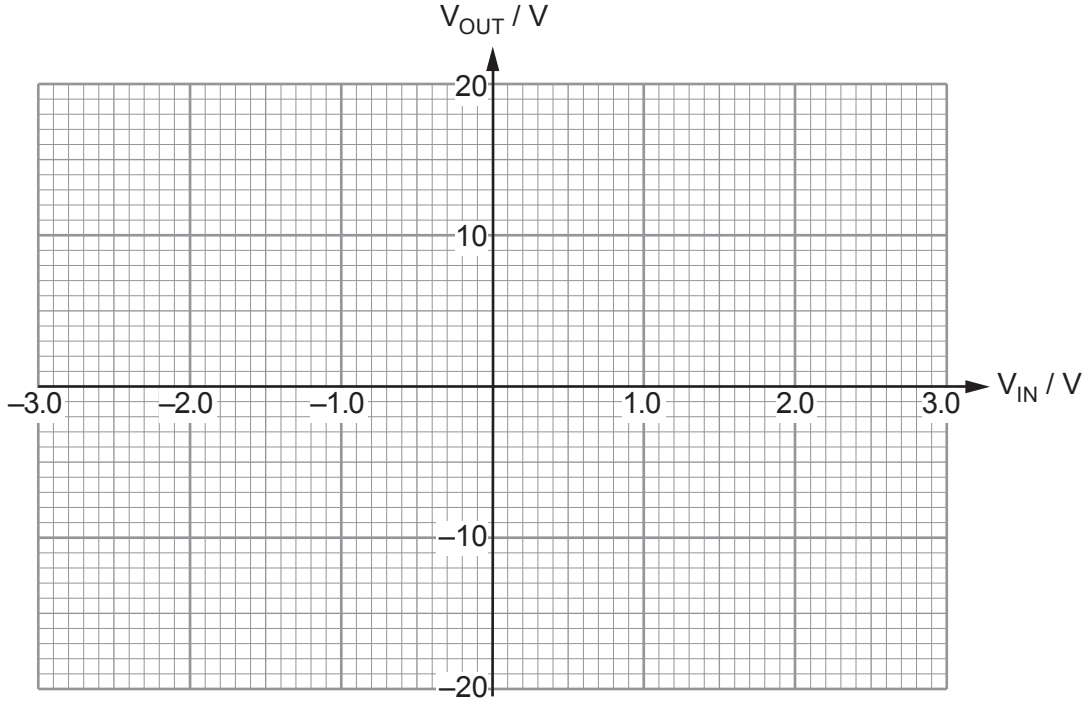
7. The following diagram shows a **non-inverting** voltage amplifier. The op-amp is powered from a ±16 V supply and the output saturates at ±15 V.



(a) Calculate the voltage gain of the amplifier and hence determine the input voltage at which the amplifier just saturates. [3]

(b) Use the information in part *(a)* to draw the graph of V_{OUT} against V_{IN} as V_{IN} is gradually increased from −3 V to +3 V DC. [3]



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(c) The voltage gain of the amplifier is changed to 12. A test signal is applied to the input of this amplifier. Use the information on the graph below to:

- calculate the amplitude of the output voltage
- label the V_{OUT} axis with appropriate values
- complete the graph to show the output voltage waveform. [3]

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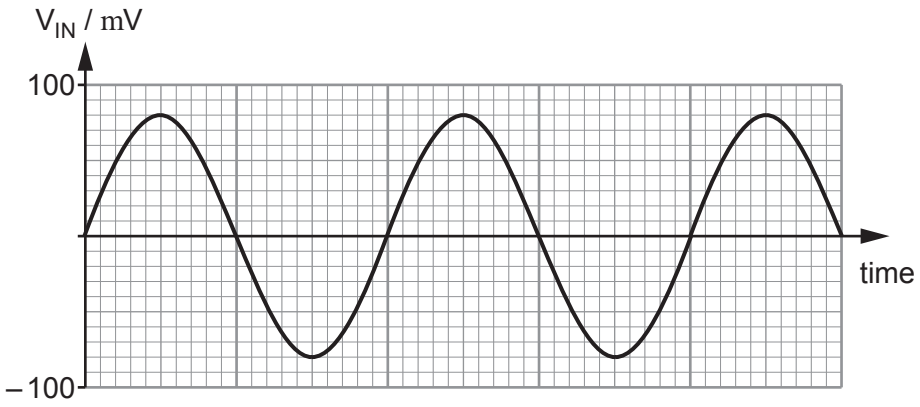

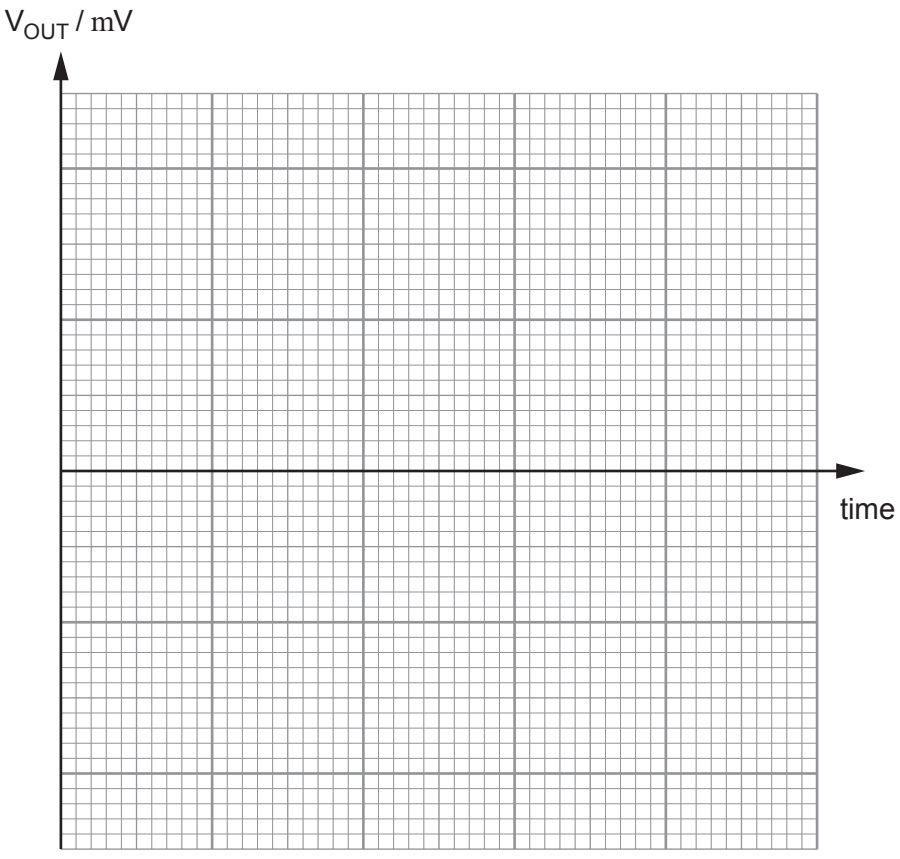

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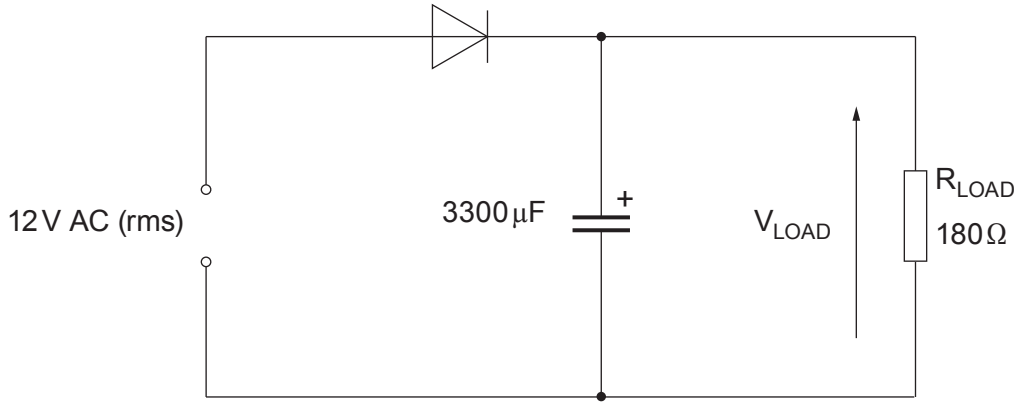
8. *(a)* The circuit for a power supply is shown below.
The AC supply is 12 V (rms), 50 Hz.



Calculate:

(i) the peak voltage V_0 of the AC supply. [2]

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(ii) the peak voltage V_{LOAD} and hence the peak load current. [3]

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(iii) the ripple voltage. [3]

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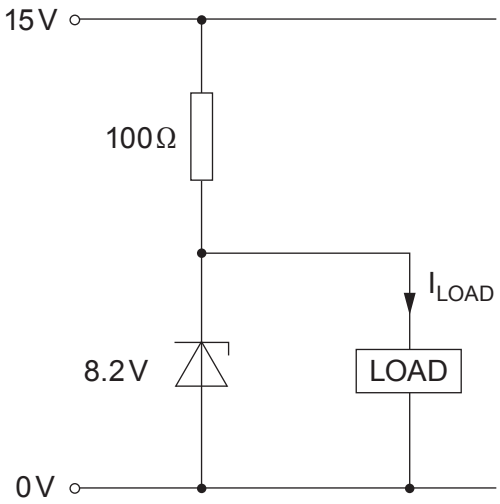
(b) A regulated power supply has the following specification:

- a stabilised output voltage of 8.2 V
- a load current of 60 mA
- when the load is disconnected the power in the Zener diode must **not** exceed its maximum power rating.



A design for the system is shown on the left.

Zener diode parameters:

V_Z =8.2 V
P_Z = 500 mW (max)
I_Z = 10 mA (minimum required to maintain the Zener voltage)

Evaluate the design against the circuit specification and suggest any changes in the design or component parameters required to meet the specification fully. [6 QER]

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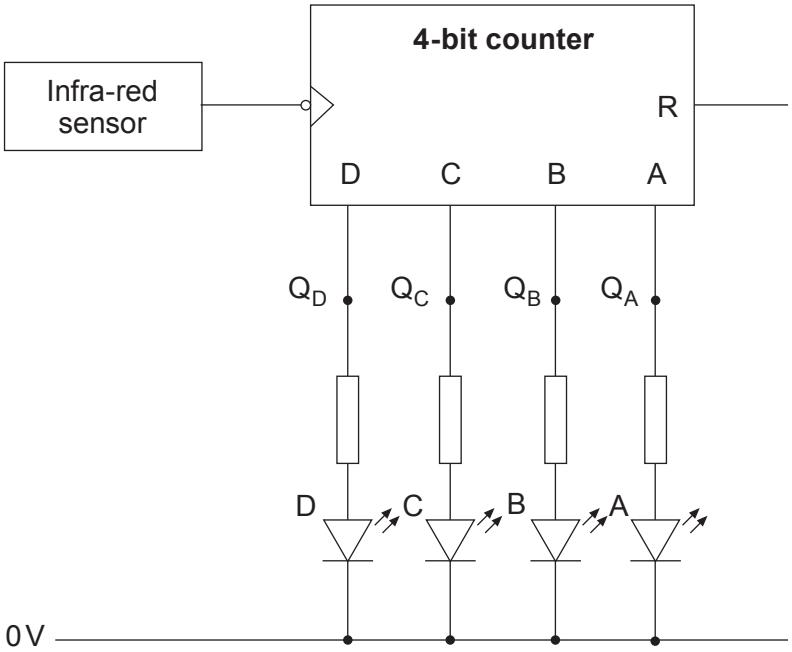
9. A system is required to count cars onto a ferry. A single pulse is produced each time a car breaks an infra-red beam. The system uses a dedicated falling-edge 4-bit counter with LEDs as the output display.



(a) Initially the ferry is empty and all the LEDs are off.

(i) How many cars have entered the ferry if LEDs A and C are on and LEDs B and D are off?

No. of cars = ...

(ii) What will be the logic levels of the Q outputs when there are 11 cars on the ferry?

Q_D = ... Q_C = ... Q_B = ... Q_A = ... [2]

(b) The ferry can carry 12 cars. On the circuit diagram add a logic gate and the connections necessary to make the counter reset on the 12th clock pulse. [3]

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(c) A different ferry uses 7-segment displays to show the number of cars loaded. The counter and display sub-system use BCD counters in place of the 4-bit binary counter. The counter/display sub-system is shown below.

(i) Explain how a BCD counter differs from a 4-bit binary counter. [1]

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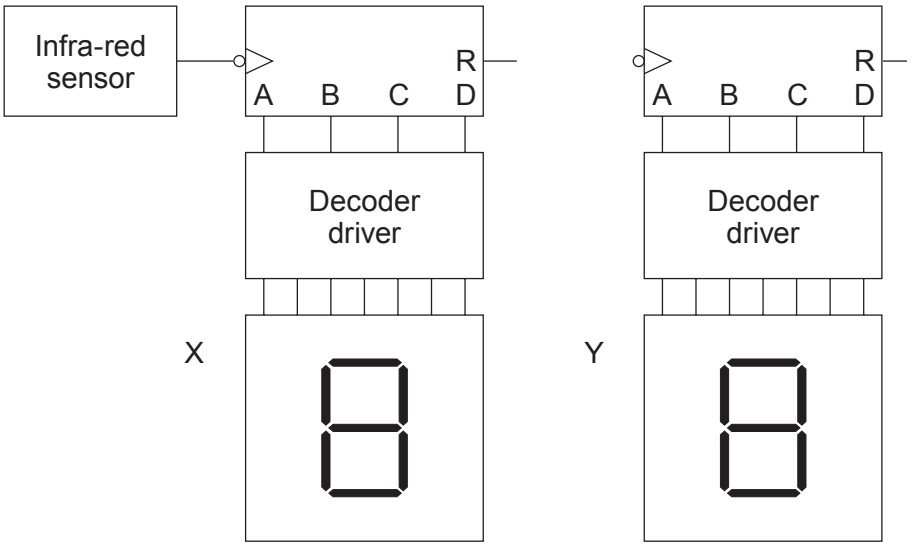
(ii) Show on the diagram how to connect the counters together. [1]



(iii) If 58 cars are loaded what number is shown on display X? [1]

.....

(d) Convert the number 58 into: [2]

(i) Binary .....

(ii) BCD .....

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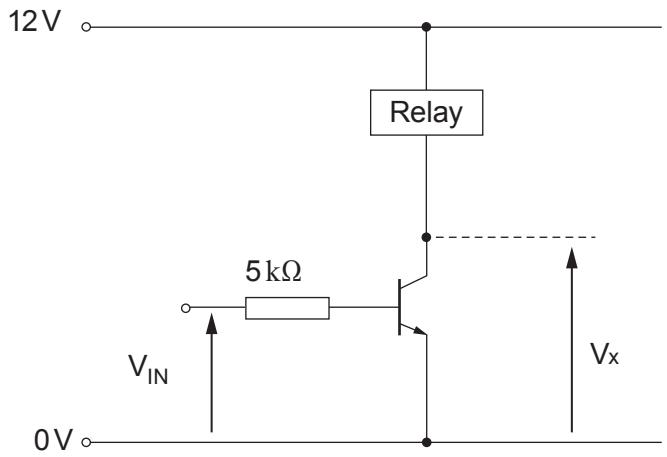
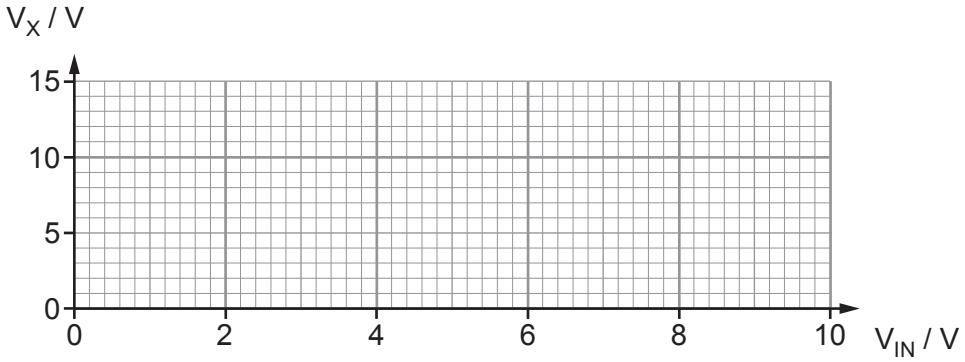
10. A transistor switch is used to operate a relay.



(a) The transistor has a current gain, h_{FE} = 60.
The relay has a resistance of 168 Ω
Calculate the value of V_{IN} that will **just** saturate the transistor. [5]

(b) (i) Draw a graph to show how V_X changes as V_{IN} is increased from 0 to 8 V. [2]



(ii) Use the graph to determine the value of V_X when V_{IN} = 3 V. [1]

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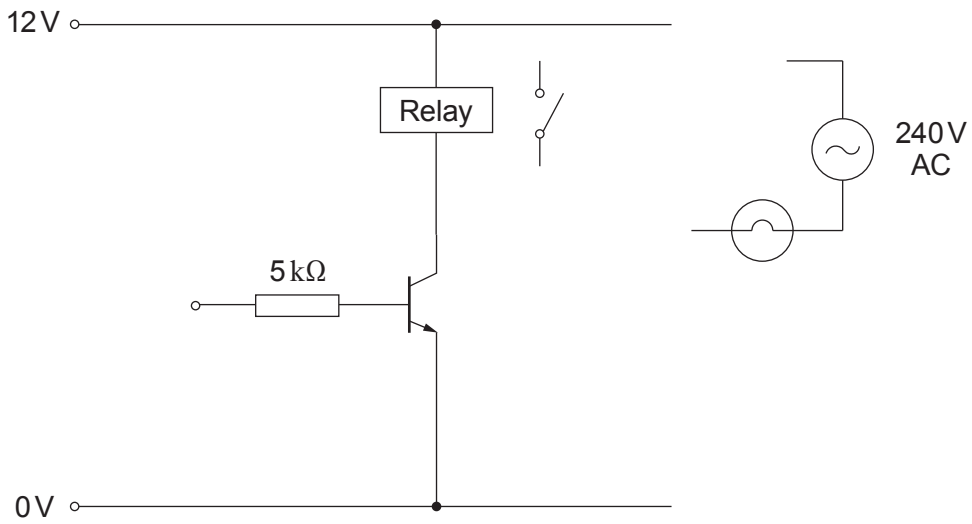
(c) Calculate the collector current and power dissipated in the transistor when V_{IN} = 3 V. [4]

(d) The switching circuit is used to control a 240 V mains light. The light is switched on automatically when it gets dark.

Complete the diagram below by adding:

- the light sensing sub-system
- a component that protects the transistor against back emf
- the secondary circuit of the relay. [4]



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11. *(a)* An extract from the data sheet for an op-amp is given below.

Parameter	Value
Open-loop gain	3.0×10^5
Input Impedance	$2.0 \times 10^{12}\ \Omega$
Saturation voltage	±15.0 V
Slew Rate	$7.5\ \text{V}\ \mu\text{s}^{-1}$
Gain-bandwidth product	3 MHz

(i) Design an inverting amplifier to give a voltage gain of – 40. Draw a fully labelled circuit diagram of your design clearly showing component values. [4]

The op-amp is powered from a ±16 V supply.

(ii) Calculate the bandwidth of this amplifier. [2]

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(b) The voltage gain of the amplifier is changed to – 30. Explain what effect this would have on the following: [3]

(i) the input voltage at which the amplifier just saturates.

.....

(ii) the bandwidth of the amplifier.

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(iii) the slew rate of the amplifier.

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(c) Describe in detail how you would determine the bandwidth of an inverting amplifier experimentally. The voltage gain of the amplifier is – 30. [6 QER]

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