Surname	Centre Number	Candidate Number
Other Names		2

GCE A LEVEL – NEW

A490U20-1

S19-A490U20-1

ELECTRONICS – A level component 2
Application of Electronics

MONDAY, 10 JUNE 2019 – AFTERNOON

2 hours 45 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**13**	
2.	**17**	
3.	**20**	
4.	**14**	
5.	**19**	
6.	**16**	
7.	**11**	
8.	**14**	
9.	**16**	
Total	**140**	

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01

ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.
Answer **all** questions.
Write your name, centre number and candidate number in the spaces at the top of this page.
Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.
The assessment of the quality of extended response (QER) will take place in question **3***(c)*.

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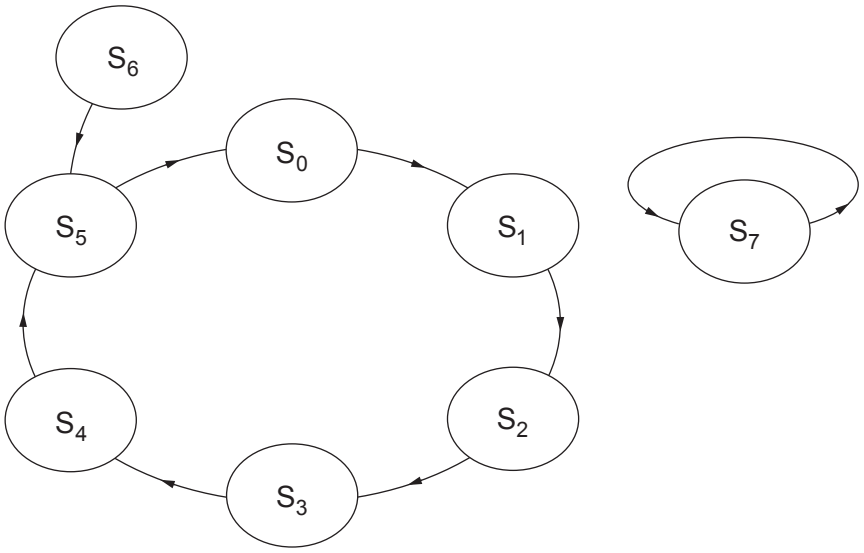
Answer **all** *questions.*

1. *(a)* The state diagram for a sequence generator is shown in the diagram:



(i) The sequence is controlled by a 2 Hz clock.
The sequence generator has been running for a while.
How long does it take to complete each cycle of the main sequence? [2]

.....

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(ii) States S_6 and S_7 are both unused. Explain the difference between them. [2]

.....

.....

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(b) Part of the truth table for a **different** sequence generator is given below:

State	Current Outputs			Next Outputs		
	C	**B**	**A**	D_C	D_B	D_A
0	1	0	1		1	
1	0	1	0		0	
2	1	0	0		1	
3	0	1	1		0	
4	0	0	0	1	0	1
5	0	0	1	1	0	1
6	1	1	0	1	0	0
7	1	1	1	1	0	0

(i) Complete the table. [1]

(ii) Write down a Boolean expression for D_B in terms of **C**, **B** and **A**. Then simplify it so that it uses only two gates. [2]

Raw expression:

D_B = ...

.....

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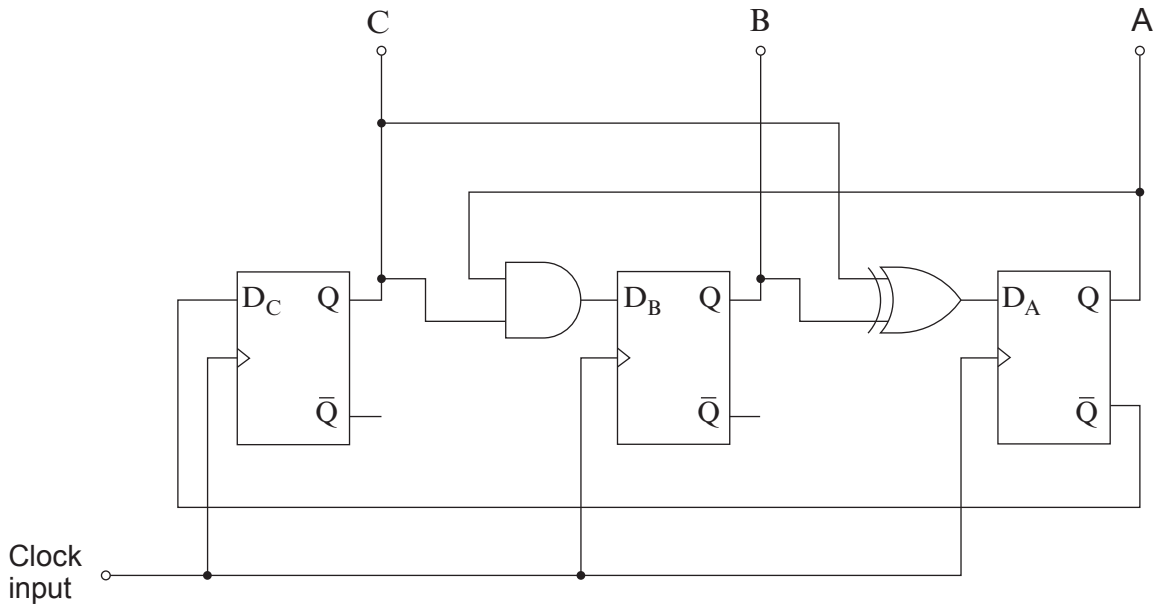
C \ BA	00	01	11	10
0				
1				

Examiner only

(c) The circuit diagram for a **third** sequence generator is shown below:



(i) Use this diagram to obtain Boolean expressions for $\mathbf{D_C}$, $\mathbf{D_B}$ and $\mathbf{D_A}$ in terms of **C**, **B** and **A**. [3]

$\mathbf{D_C}$ = ...

$\mathbf{D_B}$ = ...

$\mathbf{D_A}$ = ...

(ii) On power up, the system starts in the state **C** = 1, **B** = 0, **A** = 1.
The clock then inputs one pulse. What state is the system now in? [3]

C = ...

B = ...

A = ...

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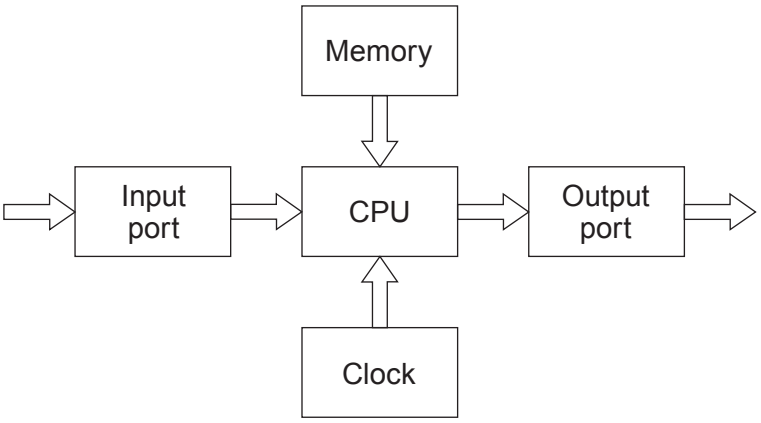
Turn over.

Examiner only

2. *(a)* The block diagram for a PIC microcontroller is shown below:



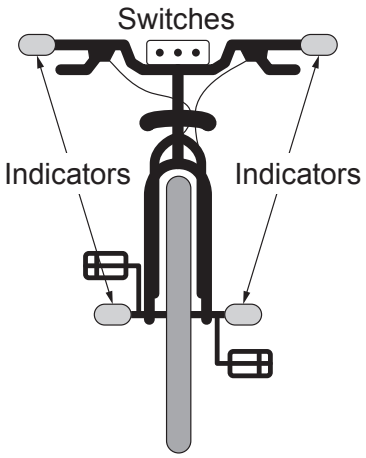
(i) Which block contains the whole program? [1]

.....

(ii) Which block has the task of synchronising data transfer and manipulation? [1]

.....

(b) A student designs a direction indicator system for a bicycle.



It has:

- four LED lamps - two, at the ends of the handlebars, pointing forwards and two, either side of the rear wheel, pointing backwards;
- three switches, mounted at the centre of the handlebars;
  - one to operate the front and rear left-hand LED lamps, to indicate a left turn;
  - one to operate the front and rear right-hand lamps, to indicate a right turn;
  - one to turn on all LED lamps as a 'hazard warning'.

When a LED lamp is switched on, it flashes at a frequency of 2 Hz.
Pressing either 'turn' switch makes the corresponding LED lamp flash ten times and then stop.
Pressing the 'hazard' switch **immediately** flashes all four LED lamps.

Examiner only

(i) The 'left-turn' switch is connected to bit 0 of the input port, PORT A.
When the switch is pressed, it outputs a logic 1 signal.

The 'right-turn switch' is connected to bit 1 of PORT A.
Again, when pressed, the switch outputs a logic 1 signal.

The program checks whether the 'left-turn' or 'right-turn' switch has been pressed.
The subroutine 'FLASH_LEFT' causes the left-hand indicators to flash on and off ten times.
The subroutine 'FLASH_RIGHT' has the same effect on the right-hand indicators.

Complete the code for that section: [5]

```
LOOP    btfsc    PORTA, .....
        call     FLASH_LEFT
        .....    .....
        call     .....
        goto     .....
```

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(ii) The following code gives the subroutine which is called to operate the left-hand LED lamps. It uses a quarter-second delay subroutine called QUART.

```
FLASH_LEFT      movwf     WSTORE
                movlw     d'10'
REPEAT          movwf     COUNT
                movlw     d'5'
                movwf     PORTB
                call      QUART
                clrf      PORTB
                call      QUART
                decfsz    COUNT,F
                goto      REPEAT
                movf      WSTORE,W
                return
```

I. Identify which port and which pins of that port are connected to the left-hand LED lamps. Explain how you arrive at your answer. [3]

.....

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II. Why are the instructions 'movwf WSTORE' and 'movf WSTORE,W' needed? [1]

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III. What value is stored in the register 'COUNT' when the program completes the subroutine and returns to the main program? [1]

.....

Examiner only

(c) (i) The 'hazard' switch is connected to cause an interrupt when pressed.
Why is it important that it is connected in this way, rather than it be polled during the main program? [2]

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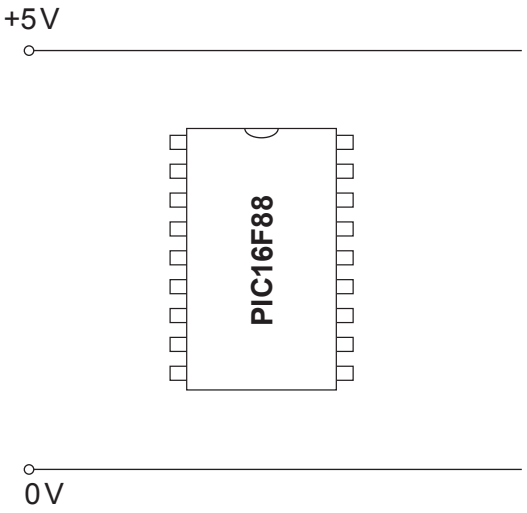
(ii) Complete the circuit diagram to show how the 'hazard' switch and any other component(s) needed are connected to the microprocessor. The switch is a 'push-to-make' type. [3]



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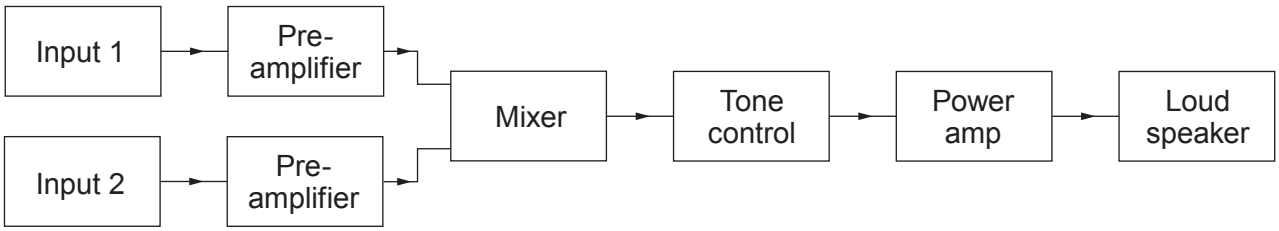
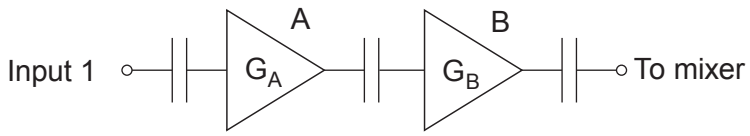
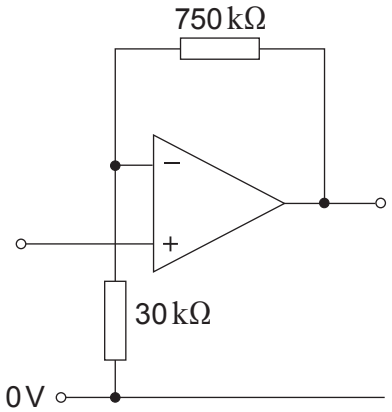
3. The following diagram shows the structure of an audio system.



(a) The preamplifier for **Input 1** consists of two non-inverting amplifiers, as the diagram shows:



The circuit diagram for each is given below:



(i) The op-amps used have a gain-bandwidth product of 3 MHz.
What is the overall voltage gain and bandwidth of the preamplifier? [5]

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Examiner only

(ii) The preamplifier includes three capacitors. What is their function in this circuit? [1]

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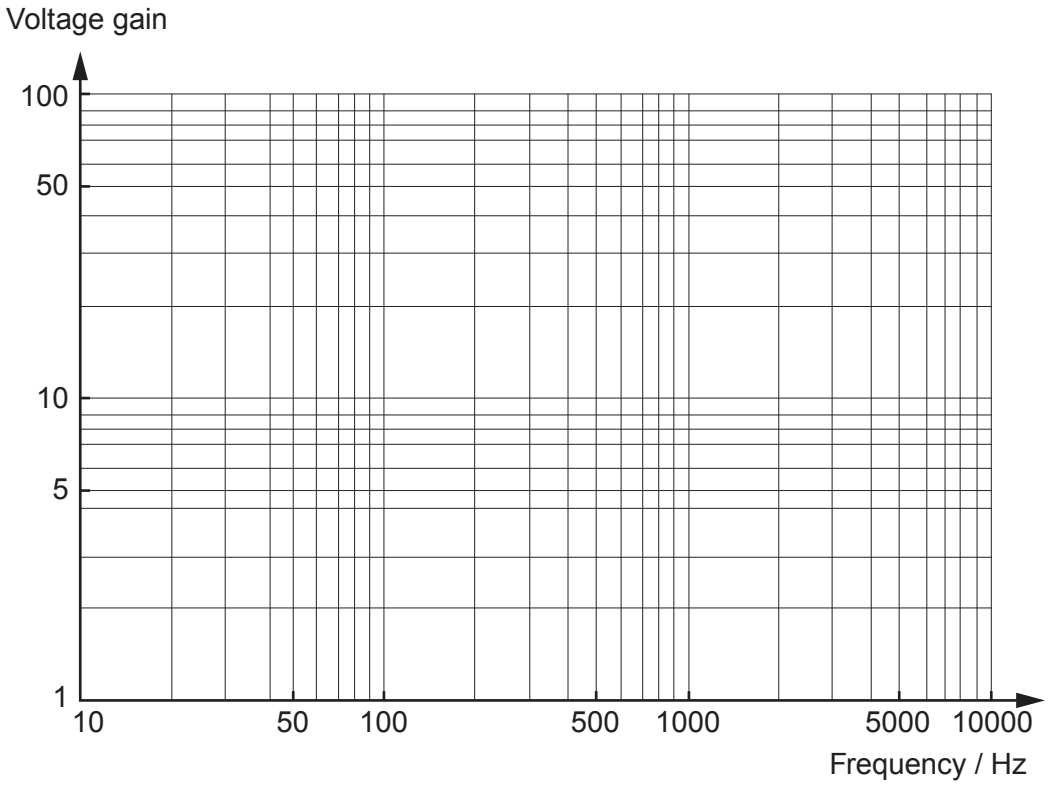
(b) A first order active filter is used in the tone control block to boost those parts of the signal with frequencies below 200 Hz.
The filter gives all frequencies above this limit a voltage gain of 2.

(i) Use this information and the axes provided to sketch the frequency response of this filter. [3]



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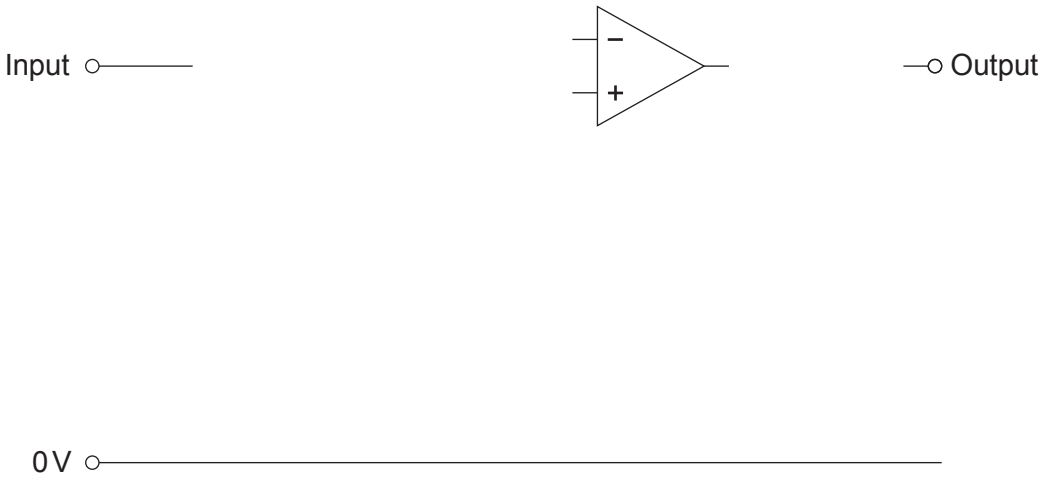
(ii) Design a suitable circuit for this filter to create the best possible fit to the specification, using the following components (and no others):

- an op-amp;
- a 39 kΩ resistor;
- a 82 kΩ resistor;
- a 10 nF capacitor.

Complete the circuit diagram for your design. [5]



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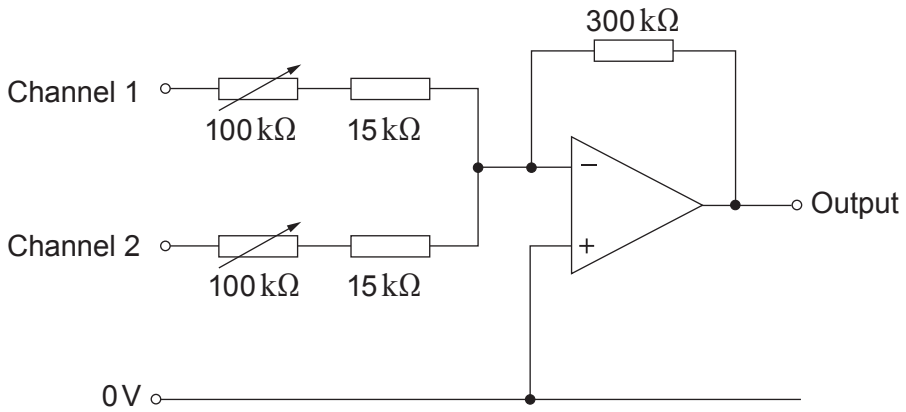
(c) Here is the specification for the audio system mixer:

Number of channels	2
Input impedance (both channels)	>10 kΩ
Voltage gain (both channels)	variable from 2× to 20×

The following circuit is proposed as a suitable solution.



Evaluate this circuit as a solution that meets the specification given above. [6 QER]

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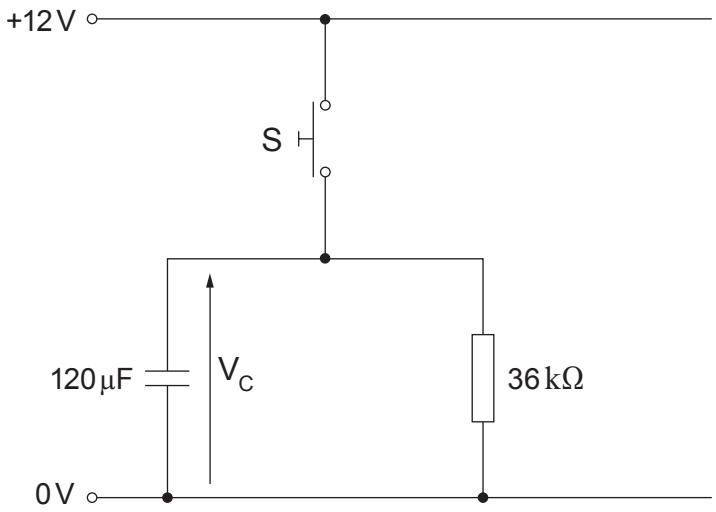
4. A shop owner wants a buzzer to sound every time someone opens the shop door.

One way to achieve this is to drive the buzzer from a NOT gate which is triggered by an input sub-system consisting of a RC network and a switch **S**, attached to the shop door frame.

(a) The RC network uses a 120 μF capacitor and a 36 kΩ resistor.
When the switch contacts close, the capacitor charges up immediately to +12 V.



(i) Calculate the time constant of the RC network. [2]

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(ii) Switch **S** is momentarily closed and then opened at time t = 0.
Determine the time taken for V_C to reach 6.0 V. [2]

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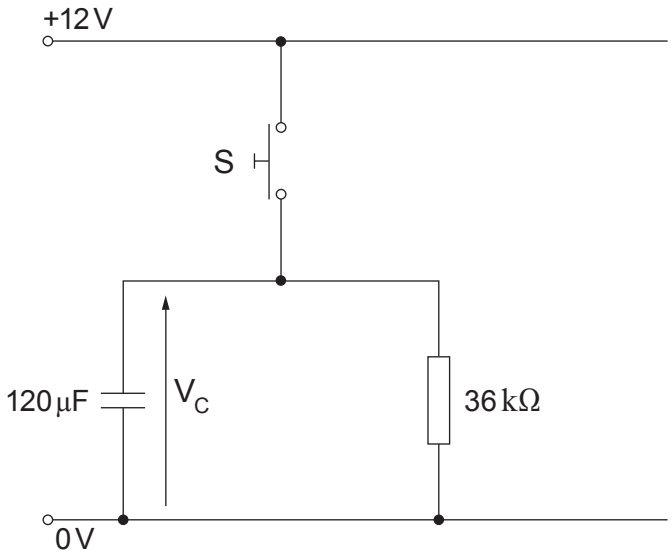
Examiner only

(b) When the shop door is closed, the switch contacts are **open**. When the door opens, the contacts **close**.

The NOT gate has a switching threshold of 6 V.

(i) Complete the circuit diagram by adding the NOT gate and buzzer. [2]



(ii) The shop door opens for five seconds, and then closes.
For how long does the buzzer sound? Explain your answer. [2]

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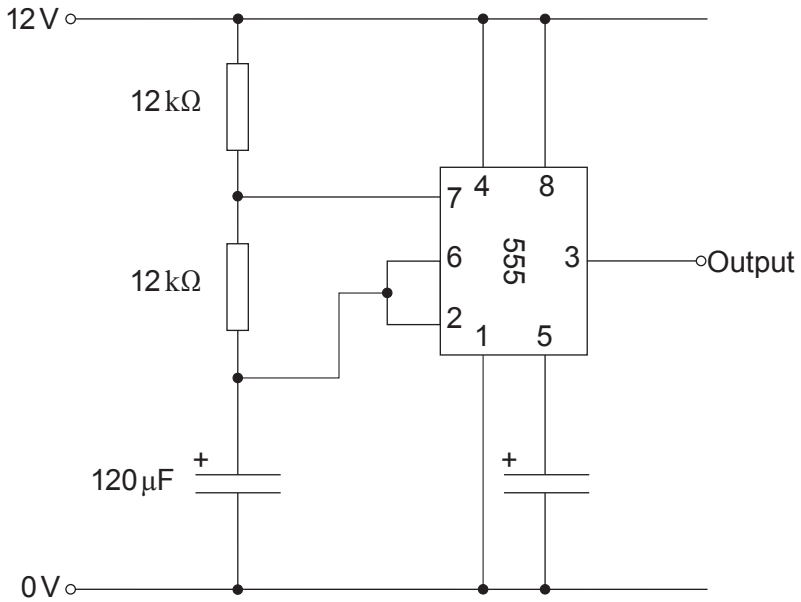
Examiner only

(c) After using the system for a while, the shop owner decides it would be more desirable to pulse the buzzer, rather than have it sound continuously.

The circuit is modified accordingly, using the astable circuit shown below.

(i) Calculate the frequency and mark:space ratio of this astable . [4]



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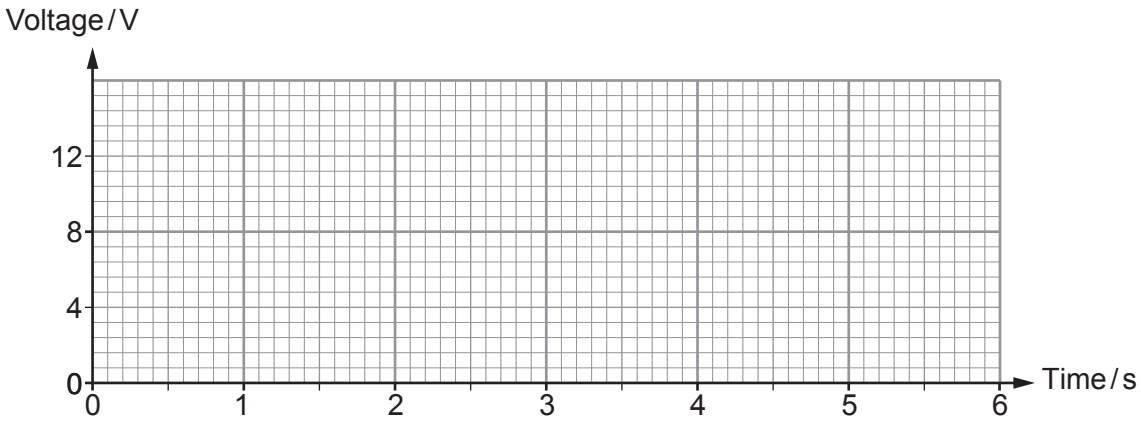
Frequency = ... Hz Mark:space ratio .....

Examiner only

(ii) Using the axes provided, sketch a graph to show **two** cycles of the output signal produced by this astable, given that it pulses between 12 V and 0 V. [2]



Examiner only

5. The following diagram shows an incomplete half-wave rectified power supply circuit.

(a) (i) The **peak** value of the transformer secondary voltage, V_{SEC}, is 21.2 V. Calculate the rms value of V_{SEC}. [2]

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.....

(ii) Complete the circuit diagram. [2]

(iii) Calculate the peak voltage of the output voltage, V_0, when the switch is open. [1]

.....

(iv) Calculate the ripple voltage when the load current is 0.2 A. [3]

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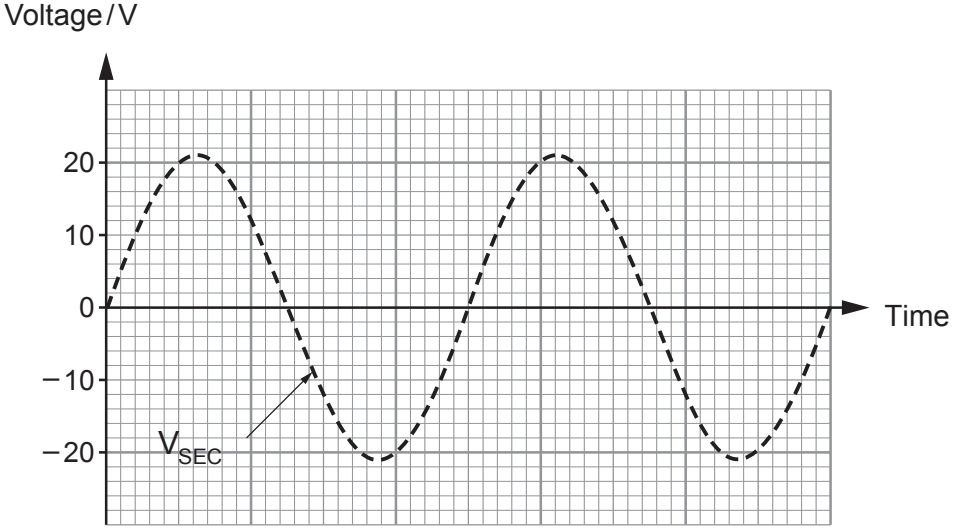
Examiner only

(v) On the axes provided, draw a graph of the voltage V_0 when there is a load current of 0.2 A. [3]

The voltage, V_{SEC}, across the transformer secondary is shown as a dashed line.



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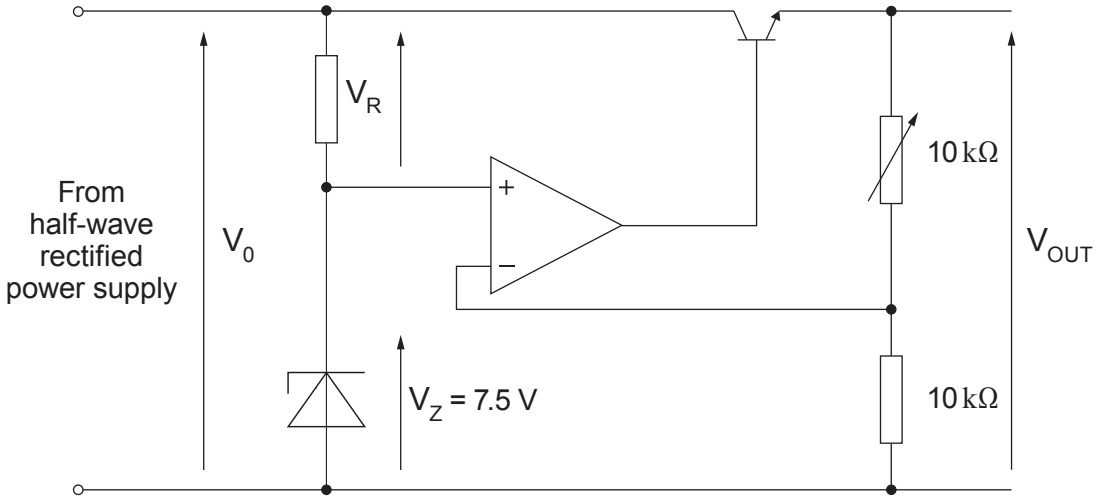
(b) By modifying the power supply as shown, it provides improved line regulation and some load regulation. It uses a 7.5 V zener diode.



(i) Complete the definitions for line and load regulation: [2]

Line regulation means that the output voltage of the power supply remains unchanged when .....

Load regulation means that the output voltage of the power supply remains unchanged when .....

(ii) Write an equation linking the quantities V_R, V_Z and V_0. [1]

.....

(iii) Explain how this circuit delivers line regulation. [2]

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Examiner only

(iv) Calculate the maximum and minimum values of V_{OUT} obtained by adjusting the variable resistor. [3]

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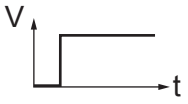
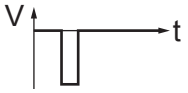
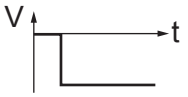
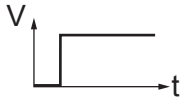
Examiner only

6. *(a)* The behaviour of a thyristor depends on the signal applied to the gate terminal and the voltage bias applied between its anode and cathode.

The table lists six combinations of these conditions, labelled **A** to **F**.

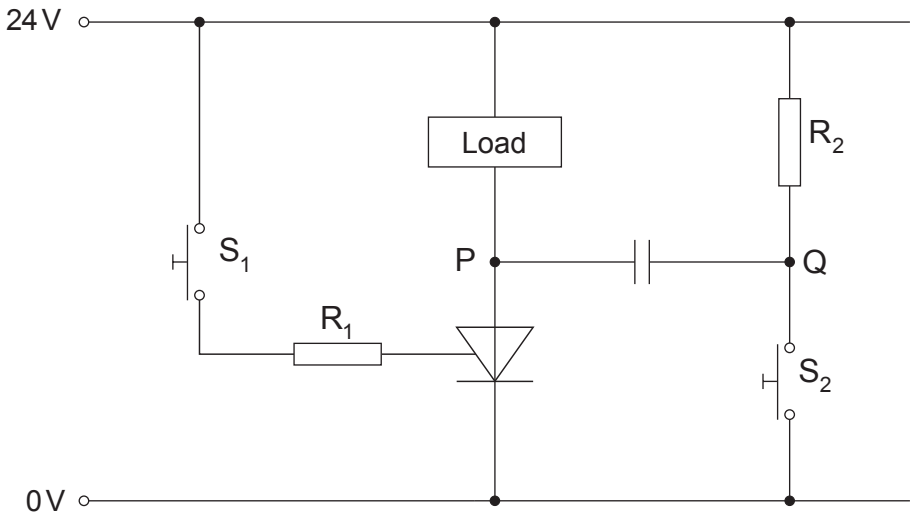
	Input to gate	Bias
A		Reverse biased
B		Forward biased
C		Forward biased
D		Reverse biased
E		Forward biased
F		Reverse biased

Select the two combinations which cause the thyristor to switch on. [2]

Combinations ..... and .....

Examiner only

(b) A high-powered DC load is controlled by a thyristor.
The circuit diagram for the control system is shown below.



(i) Here is an extract from the data sheet for the thyristor:

Characteristic	Value
Minimum gate voltage	1.2 V
Holding current	200 mA
Minimum gate current	100 mA

Calculate the maximum resistance for the resistor R_1. [3]

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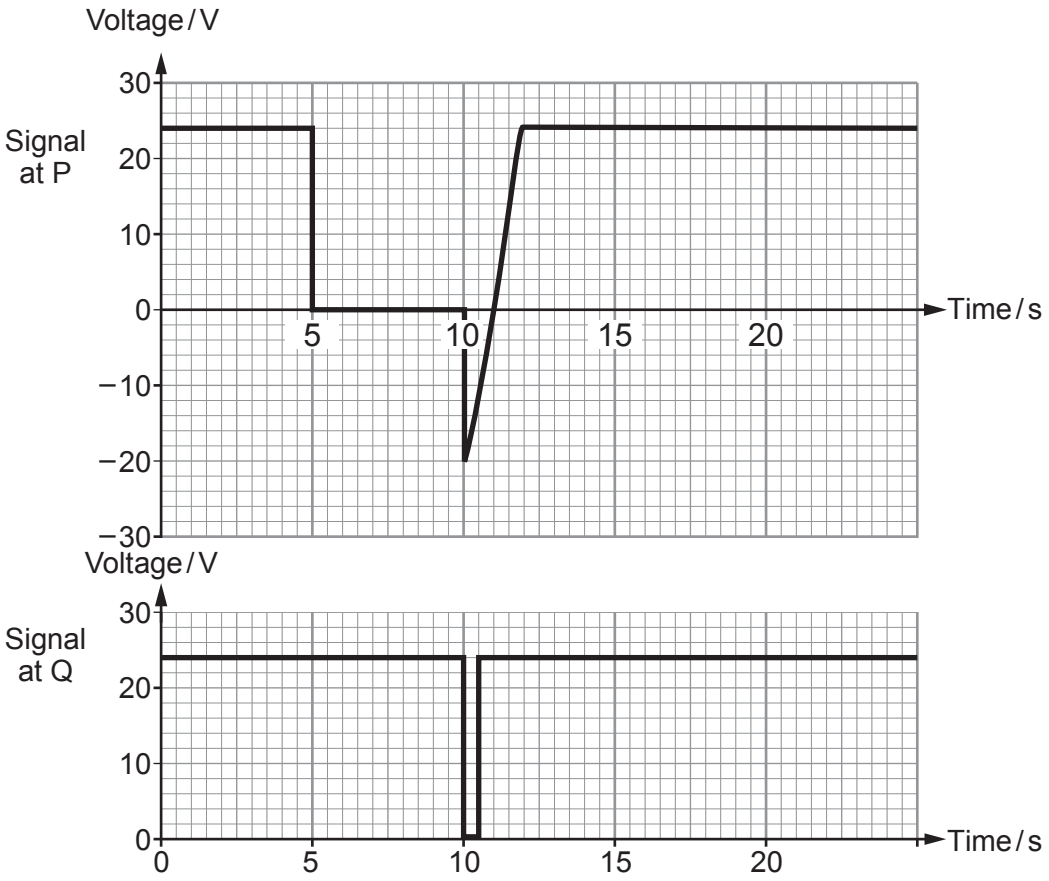
(ii) The graphs show the signals at points **P** and **Q** over a period of time:



Examiner only

Explain what is happening to the switches and to the thyristor at:

- time = 2 s; [2]

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.....

- time = 5 s; [2]

.....

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.....

- time = 10 s; [2]

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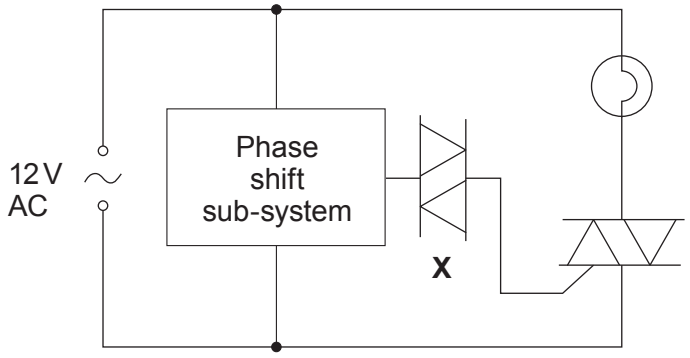
Examiner only

(c) A triac is used to control the brightness of a lamp, using a phase control sub-system. The circuit diagram is shown below:



(i) Identify component **X** and describe its function in this system [2]

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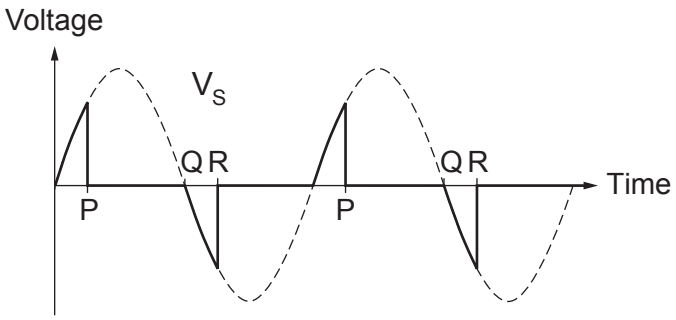
Examiner only

(ii) The graph shows the signal obtained at one point in the circuit:



I. Which component does this signal appear across? ..... [1]

II. Explain what is happening to the triac and to the lamp:

between points P and Q; [1]

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between points Q and R; [1]

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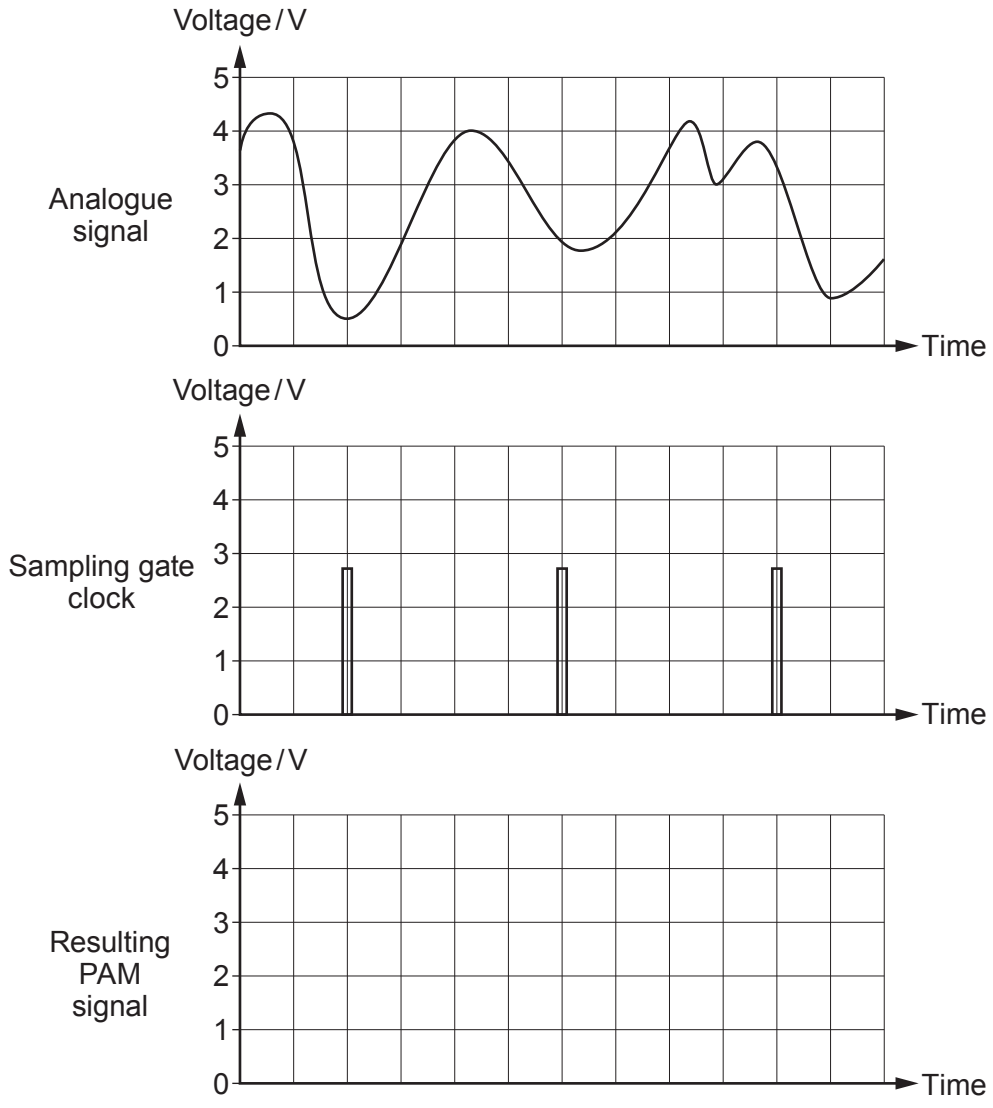
Examiner only

7. *(a)* Pulse-code modulation (PCM) is used to convert a signal from analogue into digital format, which can then be transmitted over a digital communication system.

The first part of the process is to sample the analogue signal to produce pulse-amplitude modulation (PAM).

Complete the third graph to illustrate this process for the given analogue signal and pulse train. [2]



Examiner only

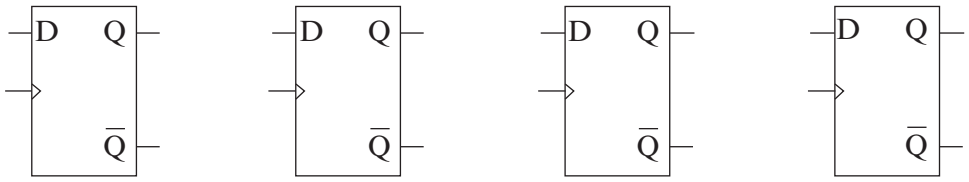
(b) Complete the block diagram for a PCM **receiver**, using the following sub-systems:

- clock;
- DAC;
- low pass filter;
- Schmitt trigger;
- SIPO shift register. [4]

Examiner only

(c) (i) Complete the circuit diagram for a 4-bit serial-in-parallel out (SIPO) shift register based on D-type flip-flops.
Data is inputted starting with the most-significant bit (msb).
Label:

- the most-significant bit (msb) of the output, **D**;
- the least-significant bit (lsb) of the output, **A**;
- the serial input of the shift register. [3]



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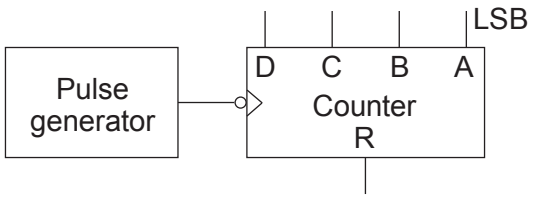
(ii) The shift register is reset so that outputs **A**, **B**, **C**, and **D** are logic 0. A logic 1 signal is maintained at the serial input.

Complete the table to show the state of the outputs as four clock pulses are applied. [2]

	Serial input	**A**	**B**	**C**	**D**
Reset	1	0	0	0	0
After one clock pulse	1				
After two clock pulses	1				
After three clock pulses	1				
After four clock pulses	1				

Examiner only

8. *(a)* The following circuit diagram shows a dedicated 4-bit asynchronous (ripple) counter.



(i) Distinguish between asynchronous (ripple) counters and synchronous counters. [2]

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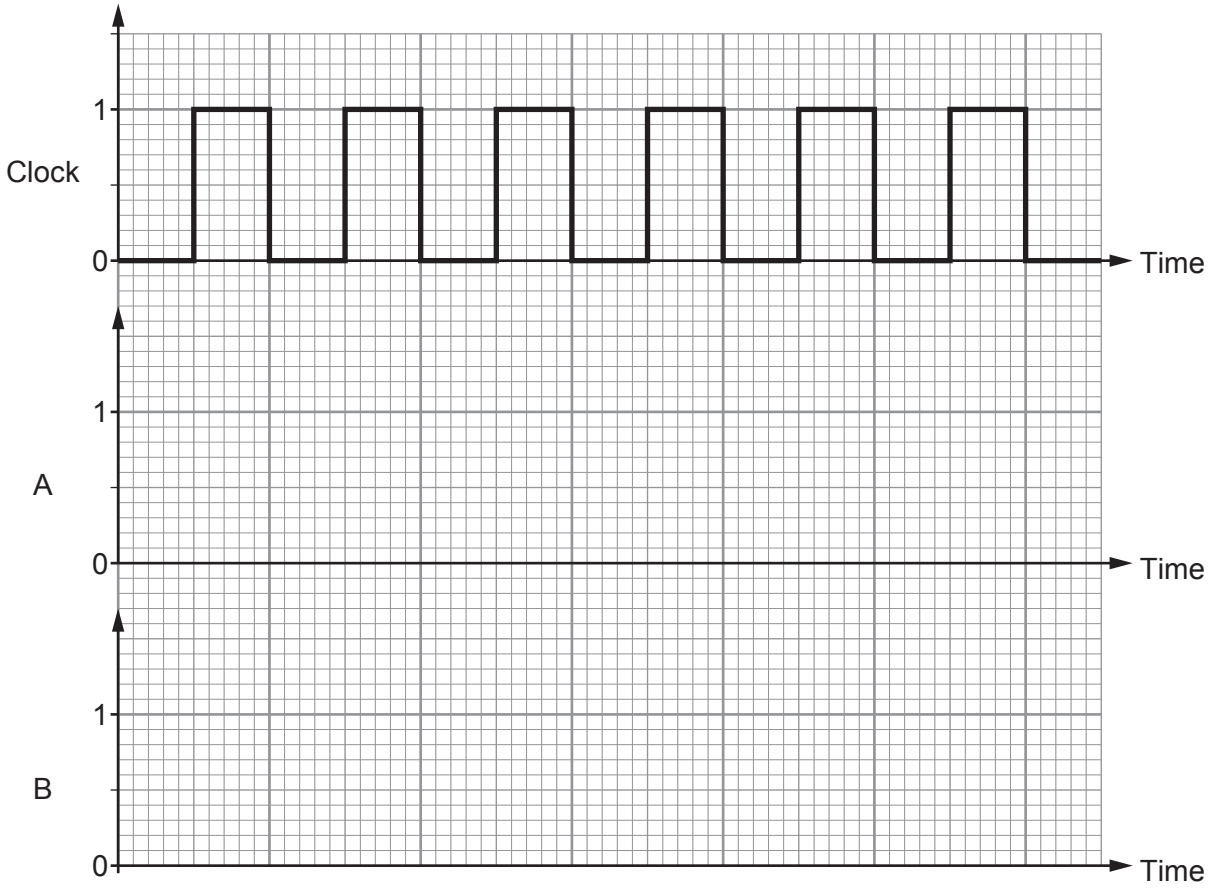
Examiner only

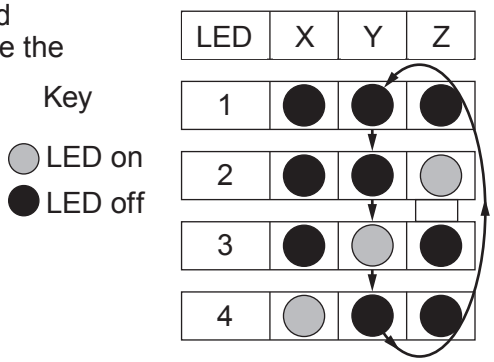
(ii) The counter is falling-edge triggered and is initially reset.

Complete the timing diagram to show the effect of the subsequent six clock pulses on counter outputs **B** and **A**. [3]



Examiner only

(b) A system based on a dedicated 4-bit counter and combinational logic system is required to produce the following light sequence:



Design the system by completing:

- the truth table; [2]
- Boolean expressions for the outputs X, Y and Z; [3]
- the circuit diagram for the system. [4]

C	B	A	X	Y	Z
0	0	0	0	0	0

.....

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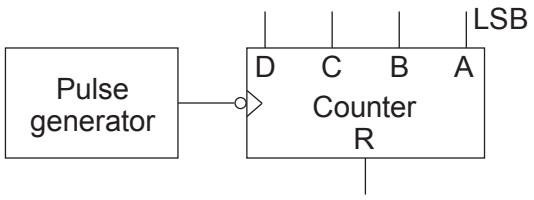

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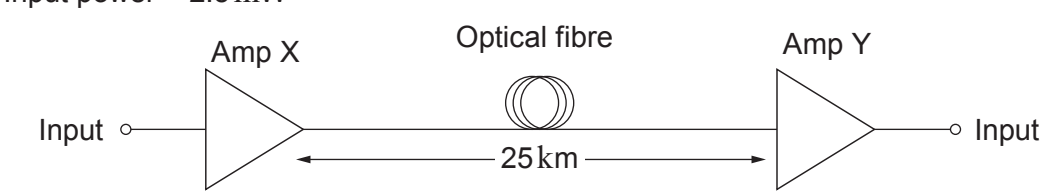
9. *(a)* Digital data is transmitted to the head office of a bank from one of its branch offices via an optical fibre link. Amplifiers X and Y are used to boost the signal amplitude.



Amplifiers X and Y both have a gain of +30 dB.
The optical fibre link has an attenuation of 2 dB km^{-1} and is 25 km long.

At the transmitter, the input power is 2.5 mW.

Calculate:

(i) the overall gain of the system in decibels; [2]

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(ii) the output power in milliwatts; [2]

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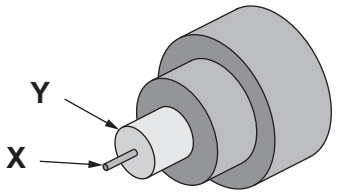
(b) The diagram shows the typical structure of an optical fibre cable.



(i) Identify the components labelled **X** and **Y**. [2]

X = ...

Y = ...

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(ii) The signal travels from amplifier **X** to amplifier **Y** using *total internal reflection*. Describe two conditions necessary for this to occur in this fibre. [2]

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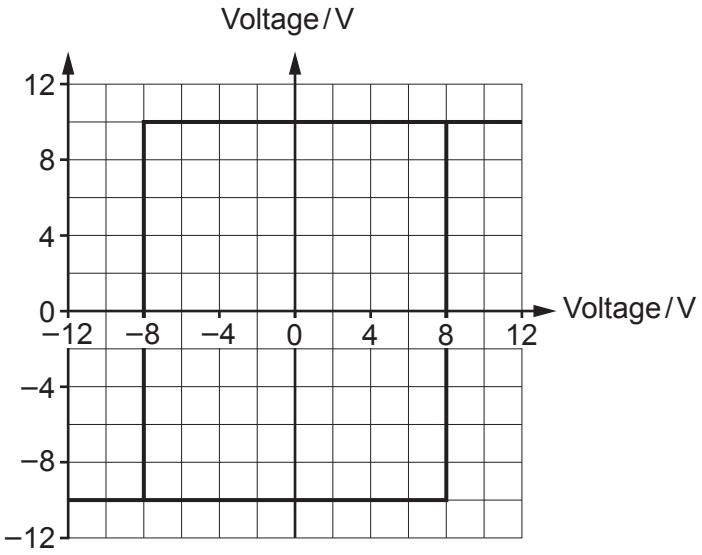
(c) The signal received at the output is converted back to an electrical signal, which is then regenerated by a Schmitt trigger sub-system.

The following graph shows the characteristics for this Schmitt trigger.



(i) Design a Schmitt trigger circuit, based on a single op-amp, that has these characteristics. [5]

Draw the circuit diagram for your design in the space below.

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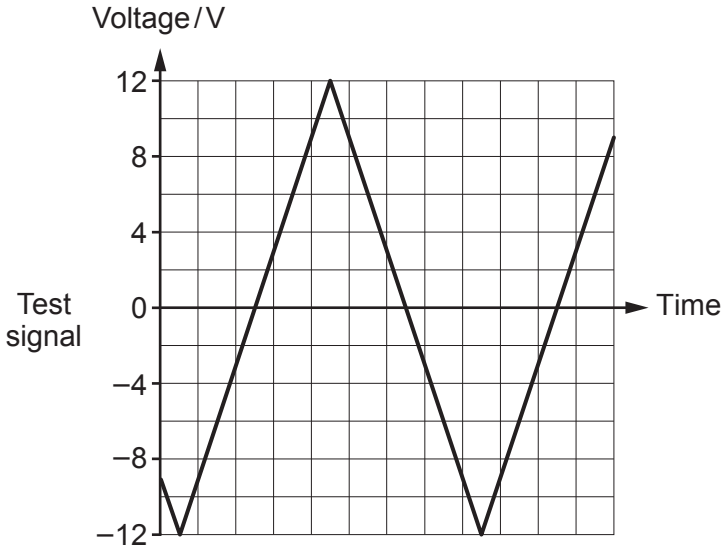
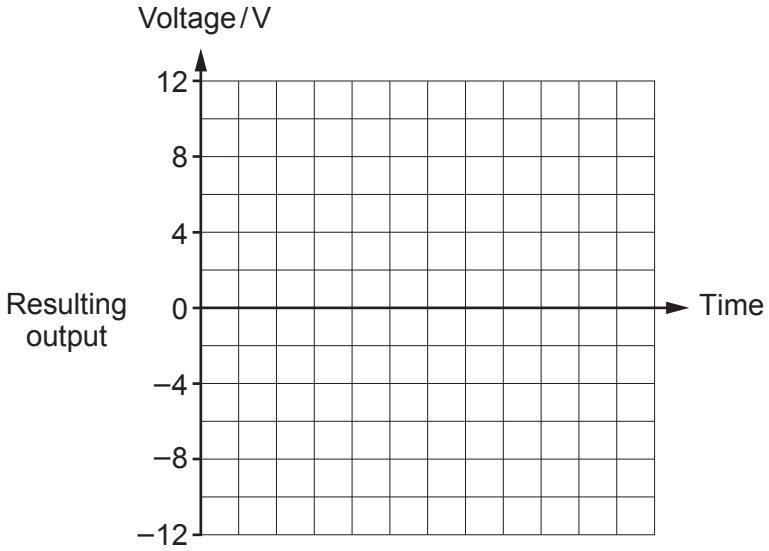
(ii) Complete the second graph to show the effect of this Schmitt trigger on the signal given in the first graph. [3]





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