GCE A LEVEL MARKING SCHEME

SUMMER 2019

A LEVEL
ELECTRONICS - COMPONENT 2
A490U20-1

INTRODUCTION

This marking scheme was used by WJEC for the 2019 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

EDUQAS A LEVEL ELECTRONICS - COMPONENT 2

MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

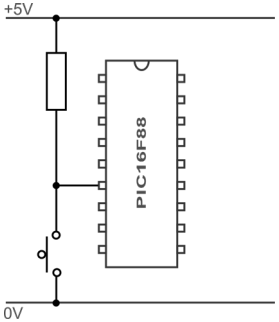
A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

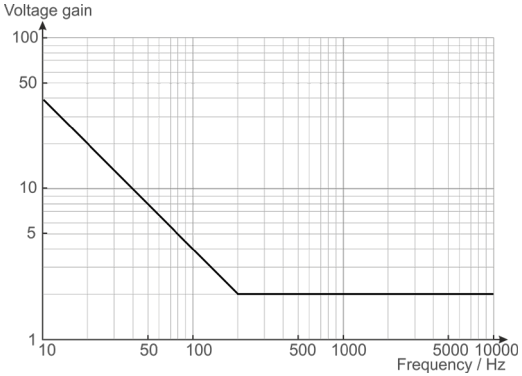
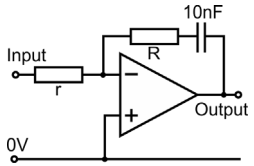
Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

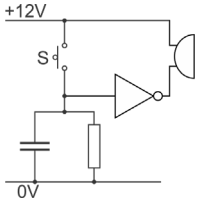
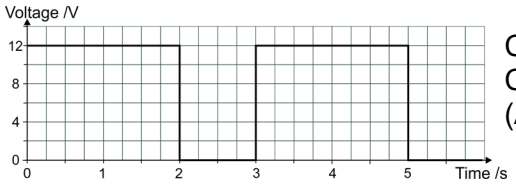
cao = correct answer only
ecf = error carried forward

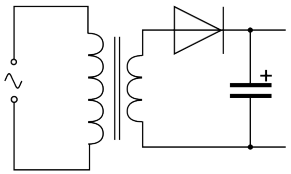
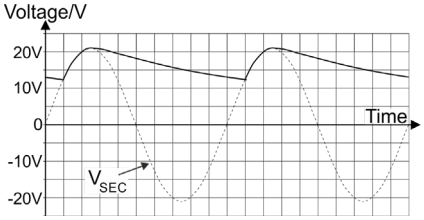
<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="5">Marks available</th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>1</td><td>(a)</td><td>(i)</td><td>No. of states in main sequence = 6
Clock period = 0.5s [1]
Time taken = 6 x 0.5 = 3s [1]</td><td>1</td><td>1</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>S6 is unused but will eventually lead into main sequence
or equivalent
S7 is a stuck state and will never allow main sequence to occur
or equivalent
Effect of unused state [1]
Effect of stuck state [1]</td><td></td><td>2</td><td></td><td>2</td><td></td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>
<table>
<tr><th></th><th colspan="3">Current Outputs</th><th colspan="3">Next Outputs</th></tr>
<tr><th>State</th><th>C</th><th>B</th><th>A</th><th>D_C</th><th>D_B</th><th>D_A</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>2</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>4</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>6</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table>
Table completely correct [1]</td><td></td><td>1</td><td></td><td>1</td><td></td></tr>
<tr><td></td><td></td><td>(ii)</td><td>$D_B = C . \overline{B} . A + C . \overline{B} . \overline{A}$ [1]
$= C . \overline{B}$ [1]</td><td>1</td><td>1</td><td></td><td>2</td><td></td></tr>
<tr><td></td><td>(c)</td><td>(i)</td><td>$D_C = \overline{A}$ [1]
$D_B = C . A$ [1]
$D_A = C \oplus B$ [1]</td><td>1</td><td>2</td><td></td><td>3</td><td>3</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>C = 0 [1]
B = 1 [1]
A = 1 [1]
ecf from c(i)</td><td>1</td><td>2</td><td></td><td>3</td><td>3</td></tr>
<tr><td></td><td></td><td></td><td>Question 1 total</td><td>4</td><td>9</td><td>0</td><td>13</td><td>8</td></tr>
</table>

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	*(a)*	i	Memory [1]	1			1	
		ii	Clock [1]	1			1	
	(b)	i	LOOP btfsc PORTA, 0 [1] call FLASH_LEFT btfsc PORTA, 1 [2] call FLASH_RIGHT [1] goto LOOP [1]	2	3		5	
		ii	I. Left-hand LEDs - bits 0 and 2 [1] In 'FLASH_LEFT', instructions 'movlw d'5' and 'movwf PORTB' turn on bits 0 and 2 of PORT B [1] as the number 5 in decimal = 0101 in binary. [1]	1	2		3	1
			II. Instructions store, and later retrieve, working register contents using the register 'WSTORE' as they may be changed within the subroutine [1]	1			1	
			III. 0 [1]		1		1	1
	(c)	i	Main program might be involved in the FLASH_LEFT or FLASH_RIGHT subroutines which last around 5s [1] whereas an interrupt gives an 'instant' response. [1]	1	1		2	
		ii	 Switch connected (high or low) [1] Resistor connected [1] Correct connection to PIC [1]	2	1		2	
			Question 2 total	**9**	**8**	**0**	**17**	**2**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	*(a)*	i	Gain of each non-inverting amplifier = 1 + 750/30 [1] Use of gain formula [1] = 26 [1] Gain of cascaded amp = 26 x 26 = 676 [1] Bandwidth = 3 000 000 / 26 = 115.4kHz [1]	2	3		5	4
		ii	Block DC signals from transferring to next amplifier stage. [1]	1			1	
	(b)	i	 High freq gain = 2 [1] Correct break frequency = 200Hz [1] Correct slope [1]	1	2		3	2
		ii	 Use of break freq. formula [1] R = 82kΩ AND r = 39kΩ [1] Capacitor in series with resistor [1] Capacitor in feedback circuit [1] Rest of circuit correct [1]	1	2	2	5	2

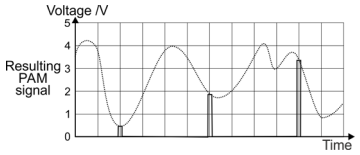
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(c)		**Indicative content:** **Number of channels -** meets the spec - two sets of input resistors. **Input impedance** - meets the spec - input resistance on each channel is 15kΩ minimum, 115kΩ maximum depending on variable resistor setting. **Voltage gain** - does not meet the spec. When variable resistor is set to zero, voltage gain = 300 / 15 = 20. When variable resistor is set to maximum, voltage gain = 300 / 115 = 2.6. **5-6 marks** A detailed analysis, including calculations, is given for all factors identified above. There is a reasoned verdict. *There is a sustained line of reasoning which is coherent, relevant, substantiated and logically structured.* **3-4 marks** A general account is given of two of the three factors involved including calculation of gain and / or input impedance for both maximum and minimum settings of the variable resistor. *There is a line of reasoning which is partially coherent, largely relevant, supported by some evidence and with some structure.* **1-2 marks** The performance of the circuit is discussed in qualitative terms only. The verdict is correct for at least two factors. *There is a basic line of reasoning which is not coherent, largely irrelevant, supported by limited evidence and with very little structure.* **0 marks** No attempt made or no response worthy of credit.			**6**	**6**	**2**
			Question 3 total	**5**	**7**	**8**	**20**	**10**

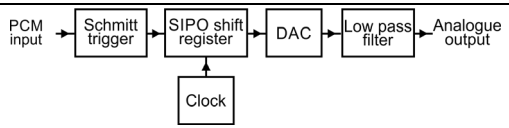
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
4	*(a)*	i	Select and use the time constant formula [1] Time constant = RC = 4.3s [1]	1	1		2	1
		ii	Use of discharge formula $t = -RC \ln(V_C / V_0)$) [1] or equivalent Time = 3.0s [1]	1	1		2	1
	(b)	i	 Correct orientation for buzzer [1] Correct connections to NOT gate [1]		2		2	
		ii	Correct calculation of half-life (3s) using 0.69RC [1] Discharge starts after five seconds. Buzzer sounds for eight seconds [1]		2		2	3
	(c)	i	Frequency = $\frac{1.44}{(12\text{x}10^3 + 24\text{x}10^3)\text{x } 120\text{x}10^{-6}}$ = 0.33Hz Evidence of correct interpretation of multipliers [1] Correct answer [1] Mark:space = $\frac{12\text{x}10^3 + 12\text{x}10^3}{12\text{x}10^3}$ = 2:1 [1] Use of formulae [1]	1	3		4	3
		ii	 Correct M:S [1] Correct period [1] (Allow e.c.f. from (c)(i))		2		2	3
			Question 4 total	**3**	**11**	**0**	**14**	**11**

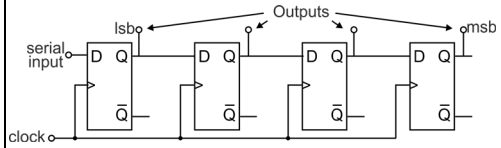
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	*(a)*	i	r.m.s. value = 21.2 / 1.4 = 15V [1] Use of formula [1]	1	1		2	1
		ii	 Diode with correct orientation to capacitor [1] Additional connections correct [1]	1	1		2	
		iii	Peak V_O = 21.2V [1]		1		1	1
		iv	Ripple voltage = 0.2 / 50 x 1000 x 10^{-6} = 4V Use of 50Hz ripple frequency [1] Use of formula [1] Correct answer [1] ecf from a(ii)	1	2		3	2
		v	 Peak value [1] Correct shape [1] Ripple voltage [1]	1	2		3	1

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	(b)	i	*Line regulation …* input (supply) voltage changes. [1] *Load regulation …* output (load) current changes. [1] or equivalents	2			2	
		ii	$V_O = V_R + V_Z$ [1]	1			1	1
		iii	Line regulation - The output voltage, V_{OUT},depends on V_Z but not on V_R . When the supply voltage changes, V_Z remains constant, V_R changes but V_{OUT} stays the same. Relationship between V_{OUT}, V_Z and V_R [1] Effect of power supply change on V_Z and V_R [1]	2			2	
		iv	When op-amp output is not saturated, both inputs sit at the same voltage, V_Z (7.5V) in this case, so voltage across 10kΩ fixed resistor = 7.5V or use of equation [1] Minimum value of variable resistor = 0Ω, so V_{OUT} = 7.5V [1] Maximum value of variable resistor = 10kΩ, so V_{OUT} = 15V [1]	1	2		3	2
			Question 5 total	**10**	**9**	**0**	**19**	**8**

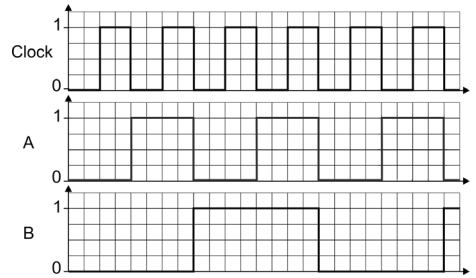
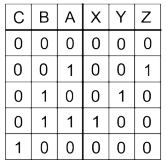
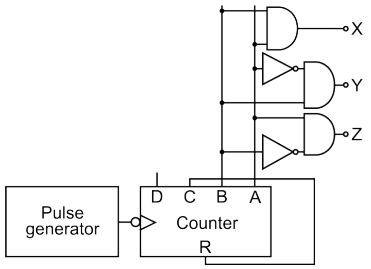
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	*(a)*		Combinations **C** and **E** - one mark each [2]	2			2	
	(b)	i	Use of min gate voltage AND current from table [1] Maximum voltage across R_1 = 24 - 1.2 = 22.8V [1] To provide minimum gate current of 100mA, maximum resistance of R_1 = 228Ω [1]		3		3	2
		ii	At time = 2s: Thyristor is off (or switch S_1 is open) Switch S_2 is oopen - one mark each [2] At time = 5s: Switch S_1 is pressed, thyristor turns on- one mark each [2] At time = 10s: Switch S_2 is pressed, Reverse biasing the thyristor Or thyristor turns off - one mark each [2] (or equivalents)		6		6	6
	(c)	i	X = **diac** [1] It improves rise time of signal triggering the thyristor to reduce the turn-on time and power dissipated in the thyristor. [1]	2			2	
		ii	I Signal appears across **triac** [1] II Between P and Q: Lamp is lit or triac is switched on [1] III Between Q and R : Lamp is off or triac is switched off [1]		3		3	3
			Question 6 total	**4**	**12**	**0**	**16**	**11**

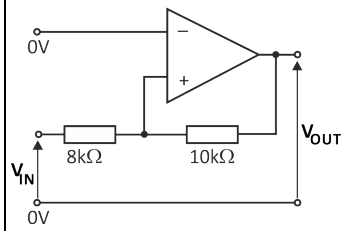
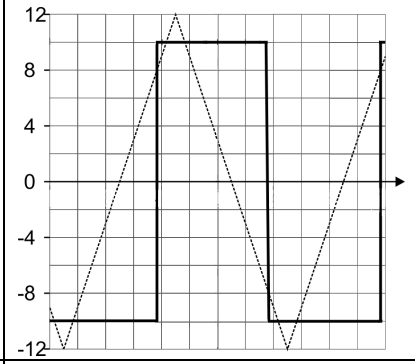
<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="5">Marks available</th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>7</td><td>(a)</td><td></td><td> 

All correct [2]
Two pulses correct - 1 mark</td><td></td><td>2</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td>(c)</td><td>i</td><td> 

All correct [4]
Three correct - 3 marks
Two correct - 2 marks
One correct - 1 mark</td><td>4</td><td></td><td></td><td>4</td><td></td></tr>
<tr><td></td><td>(d)</td><td>i</td><td> 

Q to next D (x3) [1]
Common clocks [1]
All labels [1]</td><td>2</td><td>1</td><td></td><td>3</td><td></td></tr>
<tr><td></td><td></td><td>ii</td><td><table>
<tr><th></th><th>A</th><th>B</th><th>C</th><th>D</th></tr>
<tr><td>Reset</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>After one clock pulse</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>After two clock pulses</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>After three clock pulses</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>After four clock pulses</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
All correct [2]
Only one row correct - 1 mark</td><td>1</td><td>1</td><td></td><td>2</td><td></td></tr>
<tr><td></td><td></td><td></td><td>Question 7 total</td><td>7</td><td>4</td><td>0</td><td>11</td><td>2</td></tr>
</table>

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8	*(a)*	i	In a synchronous counter, all stages are clocked at the same time from the incoming clock pulse. [1] In an asynchronous counter, stages are clocked at different times by the output of the previous stage. [1] (or equivalent)	2			2	
		ii	 Falling edge triggered [1] **A** triggered by clock [1] **B** triggered by **A** [1]	1	2		3	3
	(b)		 Rows 2 to 4 correct [1] Reset correct [1] $X = A.B$ $Y = \overline{A}.B$ $Z = A.\overline{B}$ One mark per expression [3] (allow ecf from truth table)  Output **X** correct [1] Output **Y** correct [1] Output **Z** correct [1] Reset correct [1] (allow ecf from Boolean expressions)			9	9	5
			Question 8 total	**3**	**2**	**9**	**14**	**8**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9	*(a)*	i	Overall gain = 30 - (2 x 25) + 30 [1] = 10dB [1]	1	1		2	1
		ii	Using P in dB = $10\log_{10}(P/2.5 \times 10^{-3})$ [1] Output power P = 25mW [1]	1	1		2	1
	(b)	i	**X** = core **Y** = cladding	2			2	
		ii	Refractive index of **Y** must be lower than that of **X.** [1] Angle of incidence must be greater than critical angle at the interface. [1] or equivalents	2			2	
	(c)	i	 Two correct thresholds [2] Correct circuit diagram [1] $R_{IN} = 0.8 \times R_F$ [1] Both resistors >= 1kΩ [1]	2	3		5	3
		ii	 Correct saturation voltage [1] Correct switching thresholds [1] Correct logic [1]		3		3	3
			Question 9 total	**8**	**8**	**0**	**16**	**8**

ELECTRONICS A LEVEL - COMPONENT 2

SUMMARY OF MARKS ALLOCATED TO ASSESSMENT OBJECTIVES

Question	AO1	AO2	AO3	TOTAL MARK	MATHS
1	4	9	0	13	8
2	9	8	0	17	2
3	5	7	8	20	10
4	3	11	0	14	11
5	10	9	0	19	8
6	4	12	0	16	11
7	7	4	0	11	2
8	3	2	9	14	8
9	8	8	0	16	8
TOTAL	**53**	**70**	**17**	**140**	**68**