GCE AS MARKING SCHEME

SUMMER 2019

AS
ELECTRONICS - COMPONENT 1
B490U10-1

INTRODUCTION

This marking scheme was used by WJEC for the 2019 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

EDUQAS AS ELECTRONICS - COMPONENT 1
PRINCIPLES OF ELECTRONICS

SUMMER 2019 MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

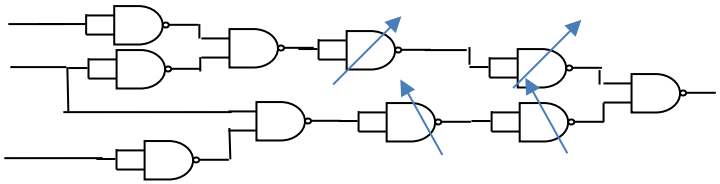
Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

cao = correct answer only
ecf = error carried forward

<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="5">Marks available</th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>1</td><td>(a)</td><td></td><td>Column Q correct (1)
<table><tr><td>B</td><td>A</td><td>Q</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table></td><td>1</td><td></td><td></td><td>1</td><td></td></tr>
<tr><td></td><td>(b)</td><td></td><td><table><tr><td>B</td><td>A</td><td>X</td><td>Y</td><td>Q</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr></table>
Column X (1)
Column Y (1) (no mark for Q)
Logic gate P = OR gate (1) (allow EXOR)</td><td>

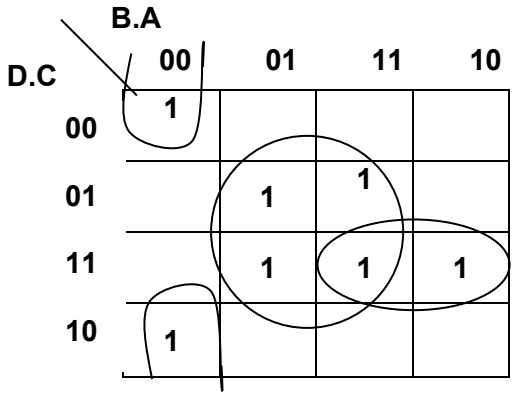
1
1</td><td>

1</td><td></td><td>3</td><td></td></tr>
<tr><td></td><td>(c)</td><td></td><td> 
NAND replacement of NOT and AND gate (both) (1)
NAND replacement of NOR gate (1)
NAND replacement of OR gate ecf (1)
Pairs of Redundant gates identified (ecf) (2)</td><td>

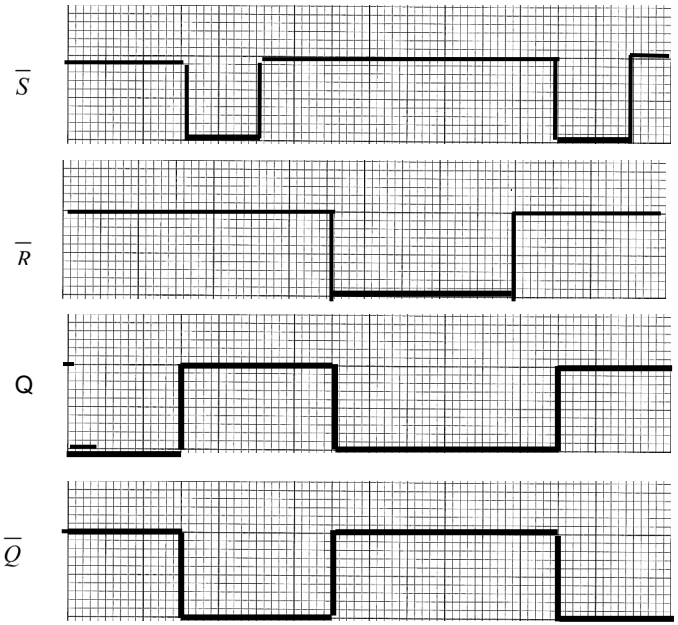
1
1
1</td><td>

2</td><td></td><td>5</td><td></td></tr>
<tr><td></td><td></td><td></td><td>Question 1 total</td><td>6</td><td>3</td><td>0</td><td>9</td><td>0</td></tr>
</table>

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	*(a)*		Method (1) either calculate $V_{threshold}$ = 16V or ratio R_{TH}/R = 5k/10k R = 6.4kΩ		1 1		2	2
	(b)		Change any fixed value resistor to a variable resistor/potentiometer	1			1	
	(c)	i	I_1 = 0 (approx.)	1			1	
		ii	(I) Selects and re-arranges formula $g_m=I_D/(V_{GS}-3)$ substitutes in equation g_M = 7.94/(6.5-3) (1) 2.27(S) (1) (II) Uses equation $r_{DSon} = V_{OUT}/I_2$ (1) 1.38/7.94 (1) 0.17 (Ω) (1) Or equivalent	1 1	 1 1 1 1		 3 3	 6
			Question 2 total	**4**	**6**	**0**	**10**	**8**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	*(a)*	i	$\overline{A}.1 = \overline{A}$ (1)	1			1	
		ii	$B.\overline{B}$ + A.B + $\overline{A}.\overline{B}$ + $\overline{A}.A$ correctly expanded brackets (1) A.B + $\overline{A}.\overline{B}$ or $\overline{A \oplus B}$ (1)	1	1		2	1
	(b)		 Correct map (1) One group of 4 and two groups of 2 identified (ecf map) (1) Any correct term from groups identified (1) Simplest overall expression (1) Q = C.A + $\overline{C}.\overline{B}.\overline{A}$ +D.C.B	1 1	1 1		4	4
	(c)		Q = $\overline{\overline{A}.\overline{B}.A + \overline{A}.\overline{B}.\overline{B}}$ (1) OR $(\overline{\overline{A}.\overline{B}}) + (\overline{A + \overline{B}})$ (1) Q= $\overline{\overline{A}.\overline{B}}$ (1) A+B + $\overline{A}.B$ either Q = A + B (1) A + B(1 + $\overline{A}$) or (1) A + B (1) Note: 1 mark for correct answer, 2 independent marks for clearly shown correct working similar to above.		3		3	3
			Question 3 total	**4**	**6**		**10**	**8**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
4	*(a)*		Correct circuit diagram (1) Correct re-arrangement R=1/fC (1) substitution R = $1/6.8 \times 10^{-6}$ (1) 147 kΩ (1)	1	 1 1 1		 4	 3
	(b)	*i*	Mark:space ratio =3:1		1		1	
		ii	Correct rearrangement $R_2 = t_L/0.7C$ $R_2 = 0.250/(0.7 \times 22 \times 10^{-6})$ =16234 Ω or 16.2 kΩ		1 1 1		 3	 3
	(c)		R_1 = 32.4 kΩ (ecf twice b(ii))		1		1	1
			Question 4 total	**1**	**8**		**9**	**7**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	*(a)*		NAND gates correctly cross-coupled and $\overline{S}$ and $\overline{R}$ connected correctly (1) LED and resistor connected between Q and 5V (1) Correct orientation of LED (1)	1 1 1			3	
	(b)		 Q goes from logic 0 to 1 on **both** falling edges of $\overline{S}$ (1) Q goes from logic 1 to 0 on falling edge of $\overline{R}$ (1) $\overline{Q}$ is the inverse of Q (1)	1 1 1			3	
	(c)		To prevent BOTH outputs going HIGH (logic 1) at the same time	1			1	
			Question 5 total	**7**	**0**	**0**	**7**	**0**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	*(a)*	*(i)*	Correct use of multipliers in any method (1) {e.g. RC =100 x 10^3 x 4.7 x 10^{-6} } 0.47 [s] (1) ln2RC = 0.326 [s] (1) {allow 0.7RC or full exponential solution}	1	 1 1		 3	 3
		(ii)	Selects and uses correct equation (1) V_C =12(1-e-(1/0.47)) (1) = 10.6V (1)	1	 1 1		 3	 3
	(b)		Circuit acts as a debounce switch (owtte) (1) Prevents multiple counts from one switch press and release (1) allow prevents miscounting	1 1			 2	
	(c)		Boxes in order: Is count = 50? (1) Delay 900 (15 min) (1) Turn turnstile on/ unlock turnstile (1) {allow Reset system}			 1 1 1	3	
			Question 6 total	**4**	**4**	**3**	**11**	**6**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7	*(a)*		9 [voltage gain = 1 + 16/2] (1) uses equation V_{IN} = 15/9 (ecf) (1) 1.67 V (1) allow 1.7V	1 1	 1		 3	 3
	(b)		Positive gradient through origin (1) Line passes through (1.0,9) (1) ecf (a) Saturates at ±15V (1)	1 1 1			 3	 3
	(c)		V_{OUT}(max) = 960 [mV] (1) Axis labelled to show peaks at ±960 mV or ±0.96 V ecf (1) Output **sinusoidal** graph with same phase and frequency as input (±0.5sq) (1)	1 1 1			 3	 1
			Question 7 total	**8**	**1**	**0**	**9**	**4**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8	*(a)*	i	*Selects and substitutes into equation* $V_0 = \sqrt{2} \times 12$ (1) 17V (1)	1	 1		 2	 2
		ii	V_{LOAD} = 16.3 V ecf (17 ecf -0.7) (1) Use of $I_{LOAD} = V_{LOAD}/R_{LOAD}$ = 16.3/180 (1) ecf 0.091 A or 91 mA (1)		1 1 1		 3	 3
		iii	Selects and substitutes into ripple voltage equation (1) Correct use of multipliers $V_r = 91 \times 10^{-3} / (50 \times 3300 \times 10^{-6})$ (1) ecf(ii) 0.55 V (1)	1	1 1		 3	 2
	(b)		**AO2 allocation**: Applies knowledge of the use of Zener diodes in electronic systems and understands the effects of loading Zener voltage regulators. 2 marks **AO3 allocation**: Analysis a problem and evaluates an electronic system to meet a given specification. Can interpret data to identify whether the specification is met. 4 marks **Indicative Content:** The Zener diode will maintain a stabilised output voltage of 8.2V provided the Zener current does not fall below 10mA. As soon as the Zener current falls below 10mA the Zener voltage will start to drop. When the Zener current nears zero the circuit becomes a voltage divider consisting of the 100Ω resistor and the load. The maximum current is 6.8/100 = 0.068A or 68mA. This is lower than the specification which requires 70 mA (60+10) OR ideal value of R = 6.8/70 = 97Ω therefore 100Ω too large to allow specification current. When load disconnected 68 (70) mA flows through the Zener giving power of 68x8.2 = 558mW (70x8.2=574mW) which is more than the Zener can dissipate and so it will fail.		2	4	6	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			Changes to meet specification: Replace 100Ω resistor with value less than or equal to 97Ω. If preferred value of 91Ω is us ed then I_R = 74.7mA and I_{LOAD} = 64.7mA. Replace zener with one of higher power e.g. 8.2 x 74.7=612.5 mW minimum. **5-6 marks** Comprehensive analysis of circuit performance measured against specification and supported by appropriate calculations on current handling and power. Conclusions drawn with reference to the evidence. There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument. **3-4 marks** Complete analysis of either current or power with calculations or partial analysis of both. Some comment on comparison between the behaviour of the circuit and the specification. There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument. **1-2 marks** Limited analysis with an attempt at least one calculation. There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument. **0 marks** No attempt made or no response worthy of credit					
			Question 8 total	**2**	**8**	**4**	**14**	**7**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9	*(a)*	*i*	5	1				
		ii	$Q_D = 1$ $Q_C = 0$ $Q_B = 1$ $Q_A = 1$	1				
	(b)		Q_D and Q_C selected (1) Two input AND gate used (1) ALL connections correct (1)		1 1 1			
	(c)	i	BCD resets automatically on the tenth pulse/ Binary counts to 15, BCD to 10 or other suitable response.	1				
		ii	D on X connected to clock on Y	1				
		iii	8		1			
	(d)	i	111010_{lsb}		1			1
		ii	0101 1000		1			1
			Question 9 total	**4**	**6**	**0**	**10**	**2**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
10	*(a)*		I_C = 12/168 (1) = 0.071 [A] 71 [mA] (1) I_B = 71/60 = 1.19 [mA] (1) V_{5k} = 1,19 x 5 = 5.95 [V] (1) V_{IN} = 5.95 + 0.7 = 6.65 [V] (1)	1 1	 1 1 1 		 5	 4
	(b)	i	Horizontal line from V_X = 12 V until V_{IN} = 0.7 (1) Sloping line to touch x-axis at 6.65 V ecf (1)	1 1			 2	2
		ii	(Graph used to determine V_X at V_{IN} = 3V) 7 .0±1 V (1)		 1		1	 1
	(c)		I_C = (12-7)/168 or V_R = 3-0.7 = 2.3 V ecf b(ii) I_B = 2.3/5000 4.6 x 10^{-4} (1) 0.0297 A = 30 mA I_C = 4.6 x 10^{-4} x 60 = 27.6 mA (1) (24-36) P_{TR} = 7 x 30 (1) ecf 210 mW (1) (192-216)		1 1 1 1		 4	 4
	(d)		Resistor and LDR (or other opt-electronic component) as potential divider at V_{IN} (1) Correct component orientation (LDR to 0V) (1) Diode connected across relay with correct orientation AC circuit connected to relay switch (1)	1 1 1 1			 4	
			Question 10 total	**8**	**8**		**16**	**11**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
11	*(a)*	*i*	Feedback resistor R_F between output and inverting input (1) Input resistor R_{IN} between input and inverting input (1) Non-inverting input connected to 0V (1) Resistor ratio 40:1 **and** both 1kΩ or greater (1)			4	4	1
		ii	use equation BW = $3x10^6/40$ (1) 75000 [Hz] 75 k[Hz] 0.075 M[Hz] (1)		1 1		2	2
	(b)	*i*	Increases (1) accept 0.5V	1			1	
		ii	Increases (1) accept 100 kHz or equivalent	1			1	
		iii	No change (1)	1			1	
	(c)		**Indicative Content:** **AO1 allocation: Demonstrates knowledge of the equipment and techniques needed to undertake the investigation. 1 mark** **AO3 allocation: Analyses the problem and designs a suitable testing procedure to determine the bandwidth of an inverting amplifier. 5 marks** • Connect the amplifier power rails to a suitable dual rail supply. • Connect the voltage input of the amplifier to a signal generator • Connect both the input and output of the amplifier to the Y1 and Y2 inputs of a duel beam oscilloscope respectively. [check both inputs are on calibrate] • Set the signal generator on a low frequency and record the frequency (or use the calibrated time base of the oscilloscope to calculate the frequency) • Measure the amplitudes of both input and output traces. • Convert these to voltages using the calibration factor(s) on the Y controls. • Calculate and record the voltage gain V_{OUT}/V_{IN} or V_{IN} constant • Repeat for a large range of frequencies (Gain < -20) • Plot a graph of voltage gain against frequency or alternative method • Determine the frequency at which the gain/V_{OUT} is 0.7 original value (-28) • This is the bandwidth for this particular voltage amplifier (Gain -40)					

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
11	*(c)*		**5-6 marks** Comprehensive description of how to set up the apparatus, the measurements to be taken (including details of instruments/techniques) and how to calculate the voltage gain and determine the bandwidth graphically. There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument. **3-4 marks** Reasonable outline of the experimental procedure attempted with some reference to what data to collect and how to use it. There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument. **1-2 marks** Some correct attempt at describing how to set up the apparatus or which measurements to take or how to calculate the voltage gain or analyse the data. There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument. **0 marks** No attempt made or no response worthy of credit.	1	0	5	6	0
			Question 11 total	**4**	**2**	**9**	**15**	**3**

ELECTRONICS AS - COMPONENT 1

SUMMARY OF MARKS ALLOCATED TO ASSESSMENT OBJECTIVES

Question	AO1	AO2	AO3	TOTAL MARK	MATHS
1	6	3	0	9	0
2	4	6	0	10	8
3	4	6	0	10	8
4	1	8	0	9	7
5	7	0	0	7	0
6	4	4	3	11	6
7	8	1	0	9	4
8	2	8	4	14	7
9	4	6	0	10	2
10	8	8	0	16	11
11	4	2	9	15	3
TOTAL	**52**	**52**	**16**	**120**	**56**