Surname	Centre Number	Candidate Number
First name(s)		2

GCE A LEVEL

A490U20-1

O20-A490U20-1

TUESDAY, 13 OCTOBER 2020 – MORNING

ELECTRONICS – A level component 2
Application of Electronics

2 hours 45 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**13**	
2.	**10**	
3.	**11**	
4.	**11**	
5.	**15**	
6.	**19**	
7.	**9**	
8.	**12**	
9.	**23**	
10.	**17**	
Total	**140**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Answer **all** questions.

Write your name, centre number and candidate number in the spaces at the top of this page.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in question **3***(b)*.

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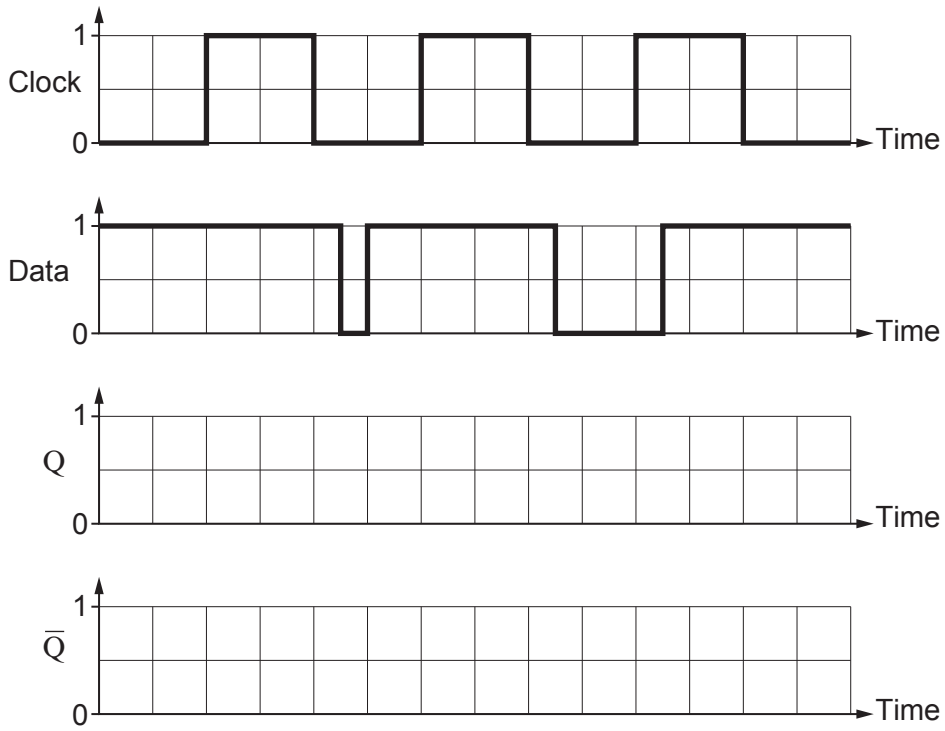
Answer **all** *questions*.

1. *(a)* The signals shown in the graphs are applied to the clock and data inputs of a rising-edge triggered D-type flip-flop. Initially, the D-type is reset.



Use the axes provided to draw the corresponding signals generated at the Q and $\overline{Q}$ outputs. [2]

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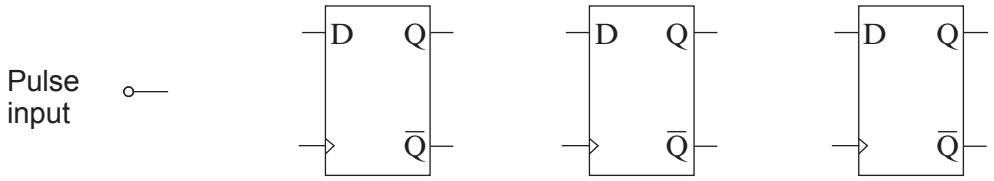
(b) (i) Complete the circuit diagram to show how three of these D-type flip-flops are connected to create a 3-bit ripple (asynchronous) binary up-counter.
Label clearly the outputs, C, B and A of the counter and the most-significant bit (MSB). [3]



(ii) What is the difference between a ripple binary counter and a synchronous binary counter? [1]

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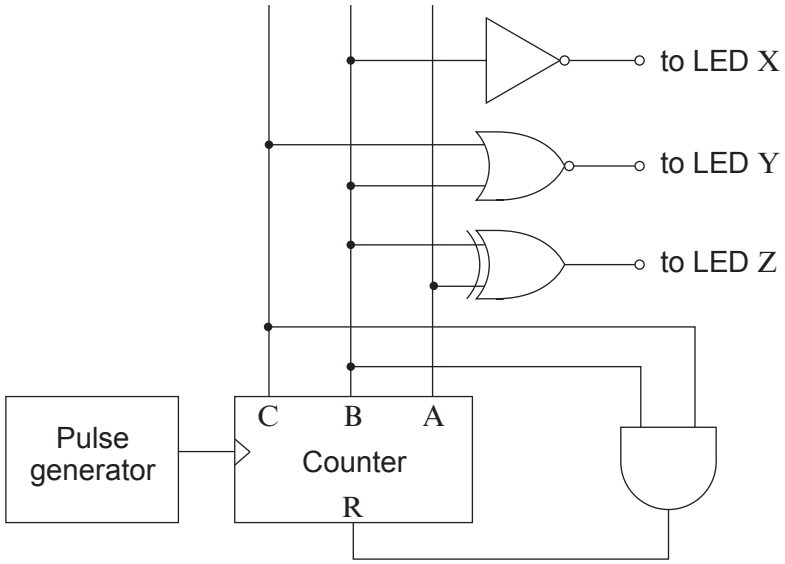
(c) A 3-bit binary up-counter, with outputs C (MSB), B and A, is used to generate a lighting sequence for three LEDs, X, Y and Z.
The circuit diagram is shown below.



Complete the truth table for the system to show the lighting sequence.
Indicate clearly where the system resets. [4]

Counter Outputs			Signals to LEDs		
C	B	A	X	Y	Z
0	0	0			
0	0	1			
0	1	0			

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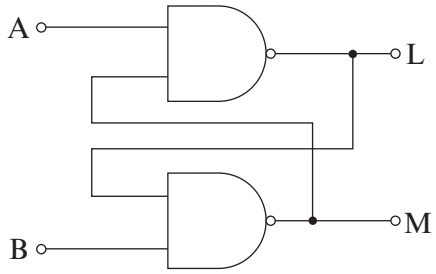
(d) The diagram shows a set-reset latch based on two NAND gates.



The sequence of signals shown in the table is applied to inputs B and A.
Complete the table to show the corresponding outputs, L and M. [3]

Step	B	A	L	M
1	0	1		
2	1	0		
3	1	1		

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2. A 3-bit sequence generator uses three D-type flip-flops. It counts down in Gray code from 111_2 and then repeats the sequence continuously.

The table shows the sequence of output states.

Current state			Next state		
C	B	A	D_C	D_B	D_A
1	1	1			
1	1	0			
1	0	0			
1	0	1			
0	0	1			
0	0	0			
0	1	0			
0	1	1			

(a) Complete the table. [1]

(b) Complete the following Boolean expressions for the inputs D_A, D_B and D_C in terms of outputs A, B and C. [4]

$D_C = C.\bar{A} +$ .....

$D_B = B.A +$ .....

$D_A =$ .....

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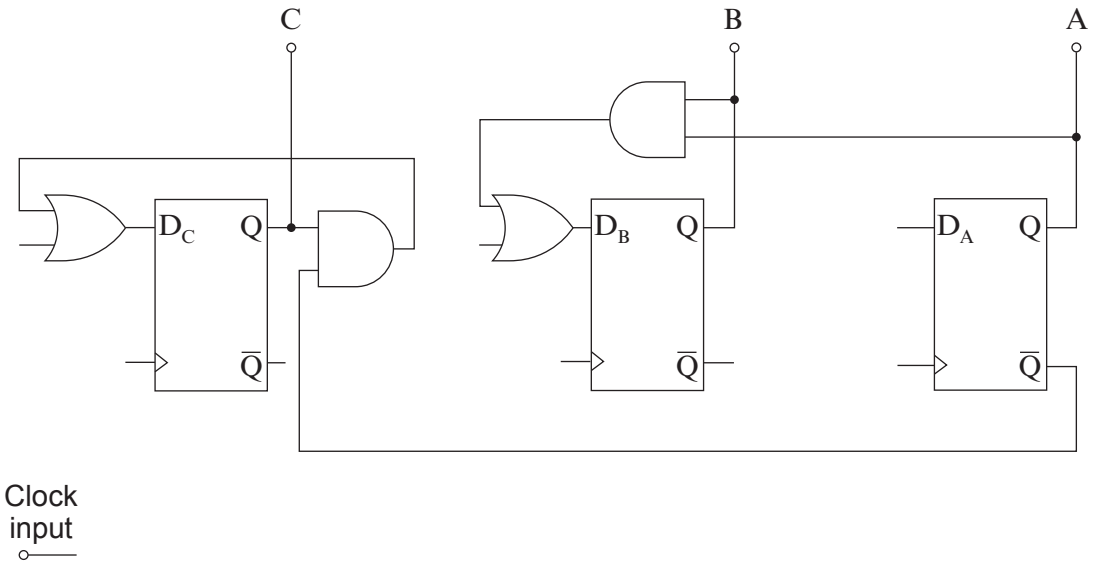
(c) Design the sequence generator. You should need to add only two extra logic gates. Complete the circuit diagram. [5]



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3. A student designs a microcontroller-based system for a quiz game to indicate which of the two teams presses its answer button first, by lighting its LED and sounding its buzzer for 2 seconds.

The selected microcontroller has two 8-bit ports, known as Port A, and Port B.

Team X has:
- a switch unit connected to Port A bit 0;
- a buzzer connected to Port B bit 0;
- a LED connected to Port B bit 1.

Team Y has:
- a switch unit connected to Port A bit 1;
- a buzzer connected to Port B bit 2;
- a LED connected to Port B bit 3.

The switch units output logic 1 signals when the switches are pressed.
The buzzers sound when they receive a logic 1 signal.
The LEDs are lit when they receive a logic 1 signal.

(a) Complete the two lines of code needed to set up Port B. [2]

movlw .....

movwf .....

(b) The main program starts at the label 'init'. It makes use of a subroutine called 'twosec' which creates a two second delay.
The program is listed below:

```
119   init    clrf    PORTB     ;reset
120   ready   btfsc   PORTA,0   ;test team X switch
121           goto    winX
122           btfsc   PORTA,1   ;test team Y switch
123           goto    ready
124           goto    winY
125   winX    bsf     PORTB,0   ;switch LED and buzzer on
126           goto    twosec
127           goto    ready
128   winY    bsf     PORTB,3   ;switch LED and buzzer on
129           goto    twosec
130           goto    ready
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Evaluate the program to see if it meets the requirements given opposite.
Suggest improvements if necessary. [6 QER]

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(c) Add three lines of code to the program below so that the teams cannot indicate an answer until the referee has pressed a switch, connected to Port A, bit 3. [3]

```
116   init     clrf    PORTB     ;reset
117   .....    .....   .....
118            .....   .....
119            .....   .....
120   ready    btfsc   PORTA,0    ;test team X switch
121            goto    winX
122 etc…..
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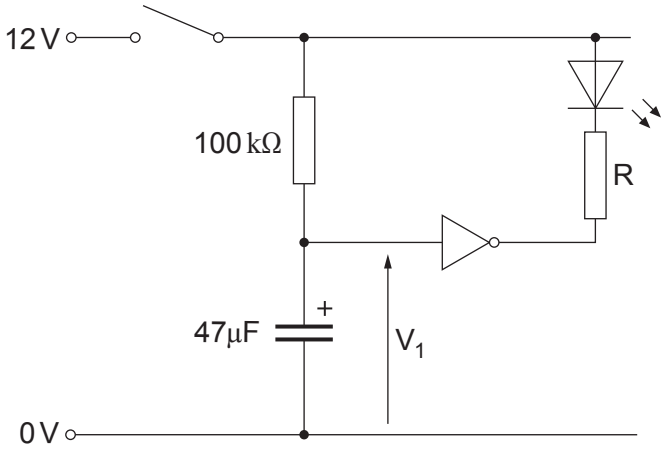
4. *(a)* A resistor-capacitor network is used in the time-delay circuit shown in the following diagram. The capacitor is initially discharged.



(i) From the time the switch is pressed, how long does it take voltage V_1 to reach 6 V? [2]

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(ii) The LED has a forward voltage drop of 2 V.
Calculate a suitable value for resistor R to limit the current through the LED to 20 mA. [2]

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(iii) The NOT gate output switches state when V_1 reaches 6 V.
The switch is pressed and held closed for 6 seconds. It is then released.

Describe the behaviour of the LED over a period of 10 seconds after the switch is pressed, giving timing information where possible. [2]

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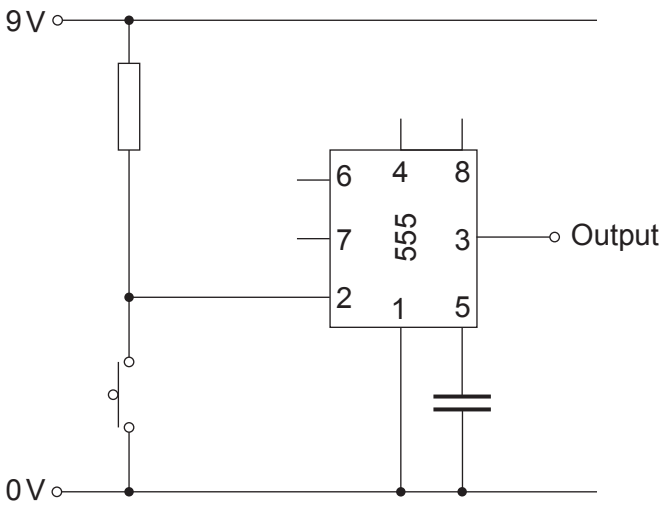
(b) (i) Complete the following circuit diagram for a 555 monostable circuit by adding:
- a resistor-capacitor network, consisting of a 100 kΩ resistor and a 47 μF capacitor;
- all connections needed. [3]



(ii) When the switch is pressed, the 47 μF capacitor starts to charge up, heading for 9 V. How long does it take to charge from 0 V to 6 V? [2]

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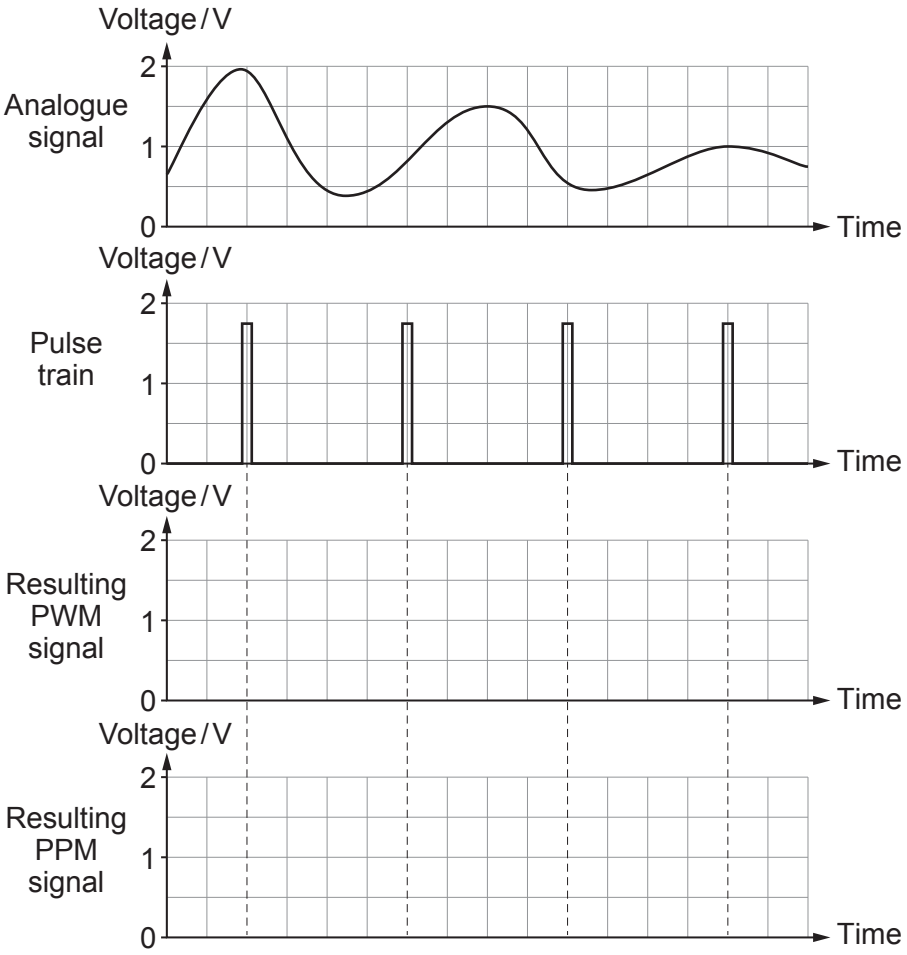
5. *(a)* In digital communications systems used to transmit audio signals, the analogue signal is used to modulate a pulse train. This can be done in a number of ways including pulse-width modulation (PWM) and pulse-position modulation (PPM).

Use the axes below to show the result of modulating the pulse train with the analogue signal using these techniques. The initial pulse timings are shown as dotted lines. [4]



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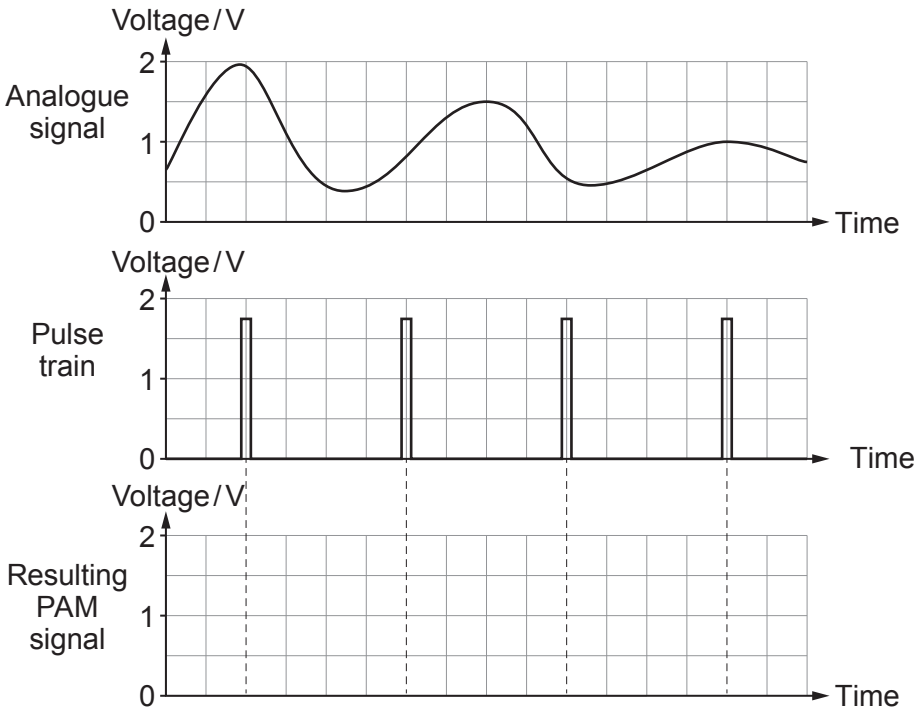
(b) In some systems, the audio signal is digitised after first converting it into a pulse-amplitude modulated (PAM) signal.

Use the axes below to show the resulting PAM signal. [2]



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(c) Time-division multiplexing (TDM) can be used to transmit digital signals from several sources along a single communications link.

Here is a description of one such system.

The system combines a number of audio signals, each with frequencies in the range 20 Hz to 4 kHz and input voltages in the range of 0 to 5 V, onto one communications link, using TDM.
It uses a sampling gate frequency of 10 kHz for all audio signals.
Each signal is converted to a 10-bit binary value.
The PISO clock rate for the system is 1.45 MHz.

(i) Why is a sampling frequency of 10 kHz suitable for this system? [2]

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(ii) What problem could arise if a lower sampling frequency were used? [1]

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(iii) Calculate the resolution of this system. [2]

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(iv) Calculate the number of these separate audio signals that can be combined in this way on this link. [4]

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6. In a pulse-code modulation (PCM) system, the analogue signal is digitised and transmitted via an optical fibre to a remote receiver.

(a) As the signal travels along the optical fibre, it is affected by *dispersion*.

Describe one cause of dispersion and explain why this causes problems in the communication system. [2]

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(b) At the receiver, a Schmitt trigger is used to regenerate the original digital signal. Describe **two** signal defects that are addressed by regeneration. [2]

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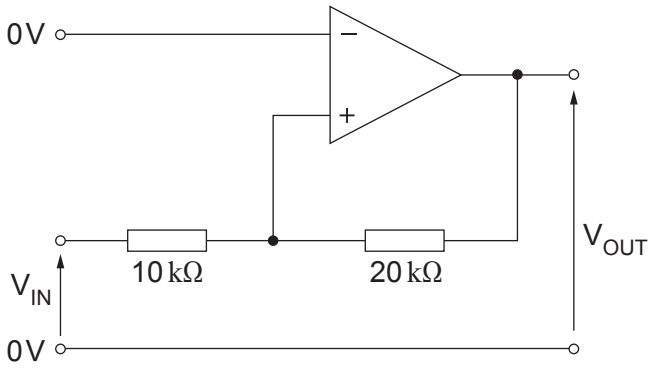
(c) The Schmitt trigger shown in the following diagram is used to regenerate a signal. The output of the op-amp saturates at +10 V and –10 V.



(i) Calculate the switching thresholds for this Schmitt trigger. [4]

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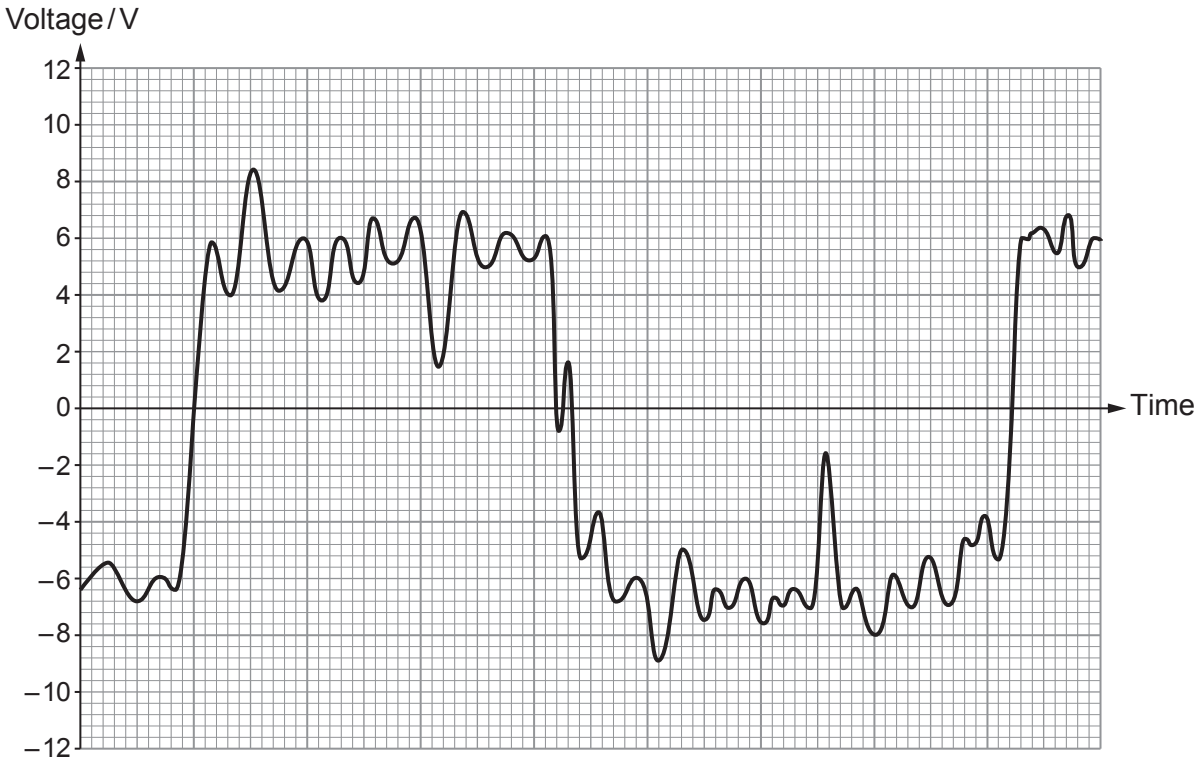
(ii) Use the axes provided to draw a graph of the output signal waveform corresponding to the input signal given. [4]



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(d) (i) The output of the Schmitt trigger is a serial stream of binary digits, representing the original analogue signal. They are assembled into four-bit data words by a SIPO shift register.

Design the shift register based on D-type flip-flops.
The sub-system should include a reset that clears the contents of the shift register. [4]

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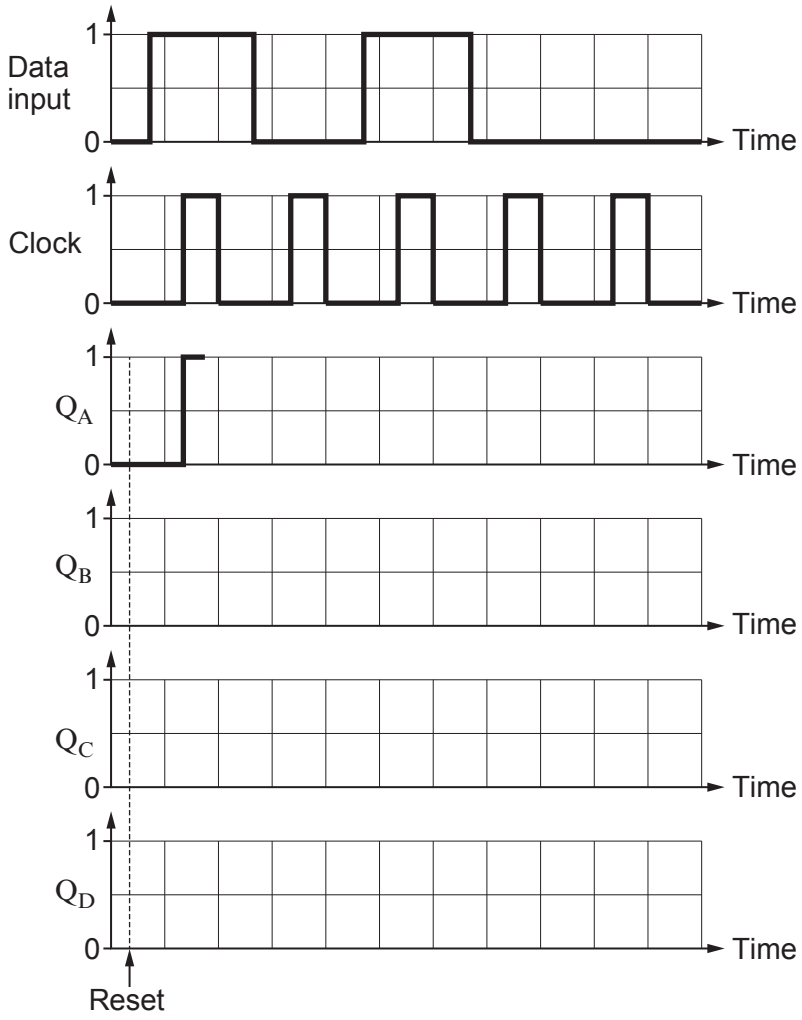
(ii) The shift register is reset at the time shown.
Complete the timing diagram for the shift register outputs, Q_A, Q_B, Q_C and Q_D. [3]



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7. *(a)* In the UK, the mains electricity supply is often described as 240 V_{rms} 50 Hz.

What is the peak value of the mains supply? [2]

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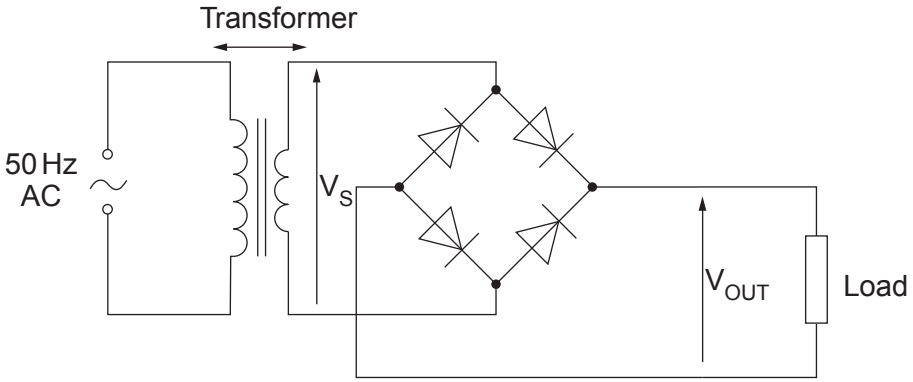
(b) The diagram shows a rectifier circuit.



The output of the transformer V_S has a peak value of 18 V.

(i) What is the peak value of the output voltage, V_{OUT}? [1]

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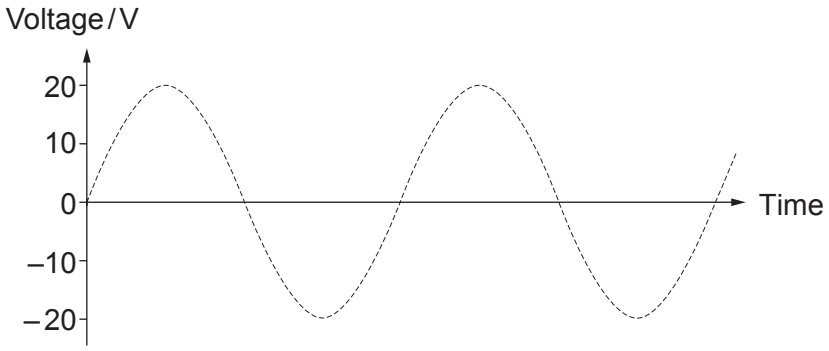
(ii) Use the axes provided below to draw the waveform of the output voltage V_{OUT}. V_S is shown as a dotted line. [2]



(iii) Modify the circuit diagram by adding a 2200 μF capacitor to smooth the output voltage. [1]

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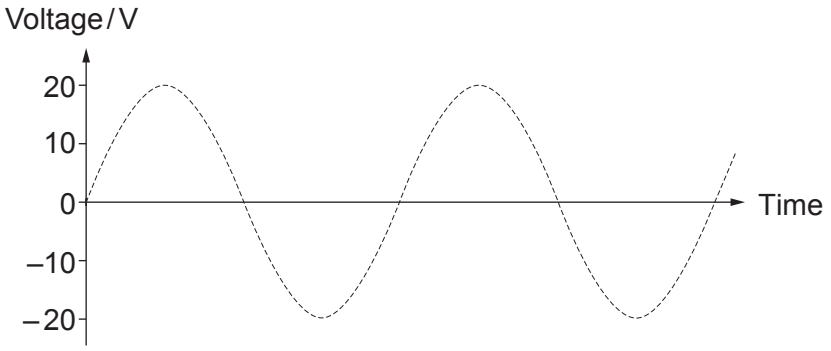
(iv) Use the axes provided below to show the effect of the smoothing capacitor on the output voltage of the circuit. [1]



(v) Calculate the size of the ripple voltage when the current through the load is 50 mA. [2]

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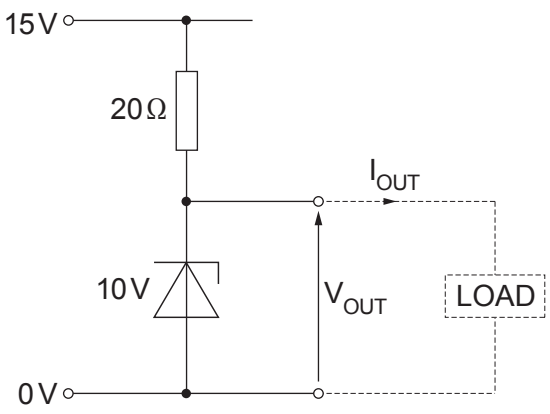
8. *(a)* The diagram shows the circuit for a simple voltage regulator, using a 10 V zener diode. The zener diode requires a minimum of 10 mA to maintain the zener voltage.



(i) What is the maximum value of output current, I_{OUT}, that can be supplied before the output voltage, V_{OUT}, starts to fall? [3]

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(ii) Calculate the minimum power ratings for the 20 Ω resistor and the zener diode. [4]

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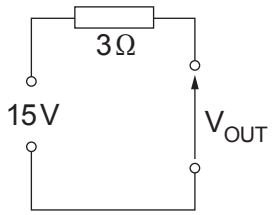
(b) A DC power supply has the Thevenin equivalent circuit shown below.



Calculate:

(i) the output current when the output terminals are short-circuited; [2]

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(ii) the load resistance that produces an output voltage, V_{OUT}, of 10 V. [3]

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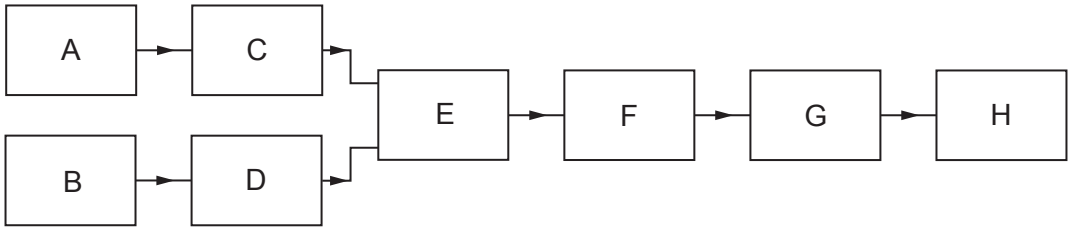
9. *(a)* In the following block diagram for an audio system, which letter identifies a:

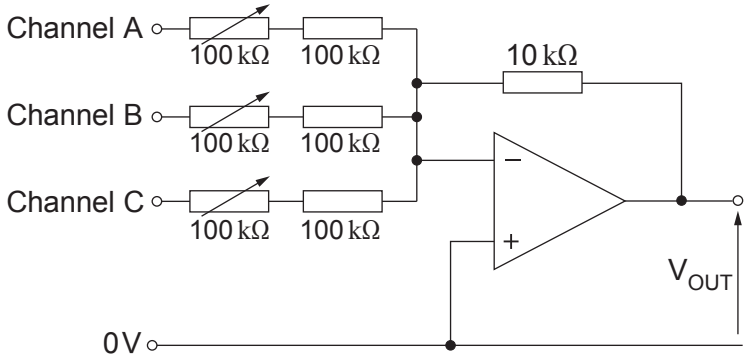
(i) mixer; .....

(ii) pre-amplifier; .....

(iii) power amplifier? ..... [3]



(b) The circuit diagram for a mixer is shown below:



(i) The output of the op-amp is not saturated.
What is the voltage at the inverting input of the op-amp? [1]

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(ii) The mixer is tested by applying a steady voltage of +5 V at each of the inputs, A, B and C and then adjusting the variable resistors.

What is the maximum theoretical value possible for V_{OUT}? [3]

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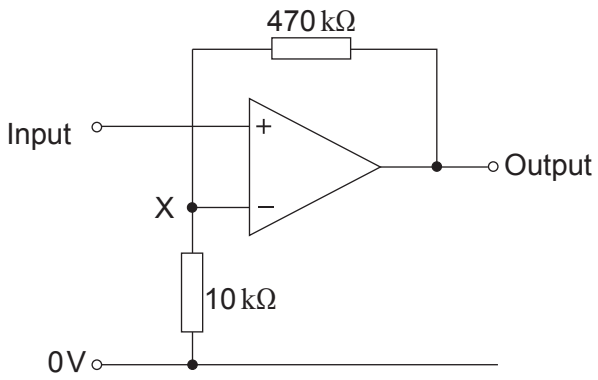
(c) The pre-amplifier circuit diagram is shown below:



The output of the op-amp saturates at ±12 V.

(i) Why is a non-inverting voltage amplifier preferred to an inverting voltage amplifier for this application? [1]

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(ii) An AC signal with amplitude of 0.17 V is applied to the input.
What is the amplitude of the output signal? [2]

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(iii) What is the voltage at point X at the instant when the input is +0.12 V? [1]

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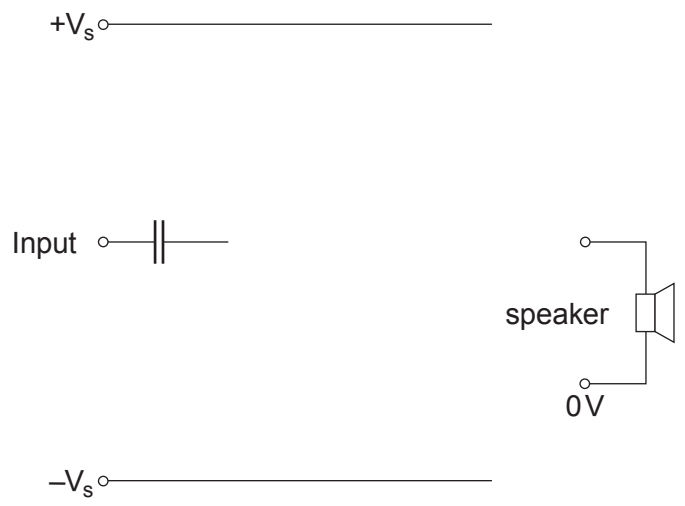
(d) (i) Use the outline provided to draw the circuit diagram for a MOSFET push-pull source follower power amplifier. [3]



(ii) What is the function of the capacitor in this circuit? [1]

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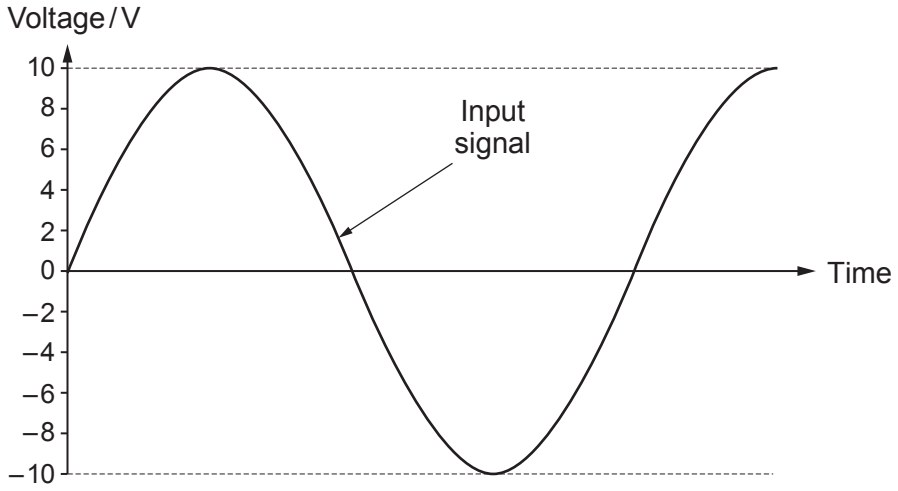
(iii) Illustrate the meaning of crossover distortion by adding to the axes a graph showing the output waveform for this power amplifier when the input signal shown is applied to its input. Label all significant voltages. [3]



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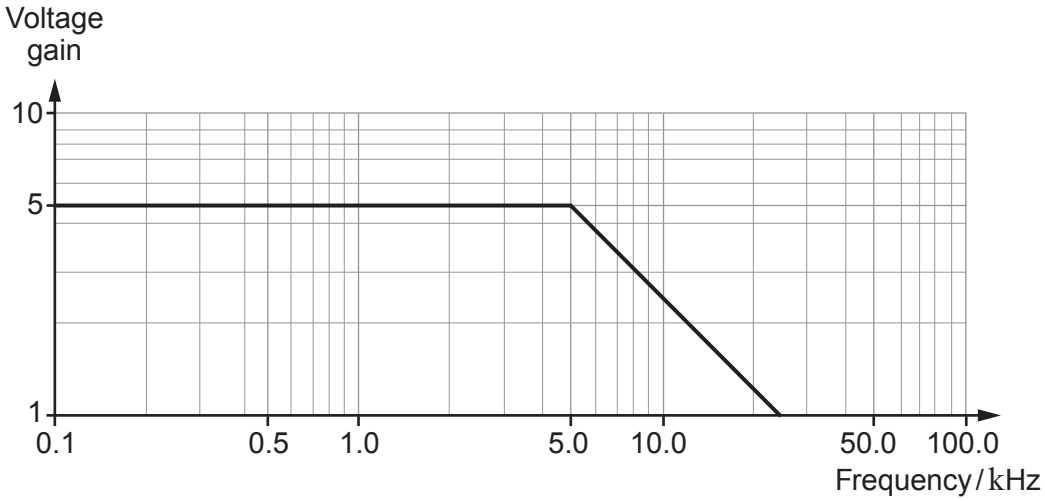
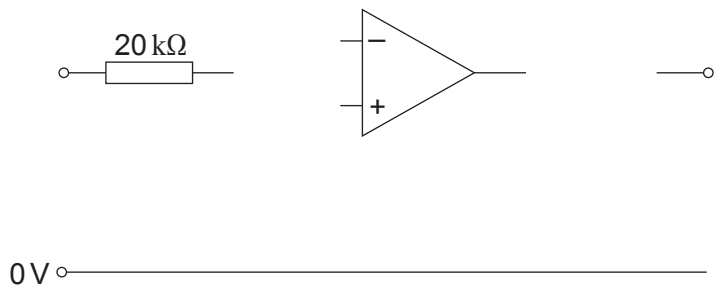
(e) The audio system incorporates a tone control consisting of an active filter with the following characteristics:



Design a suitable circuit, based on a single op-amp. [5]
Use the following template to show your design and label all components.



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10. *(a)* State one advantage of using a thyristor instead of an electromagnetic relay to switch a DC current. [1]

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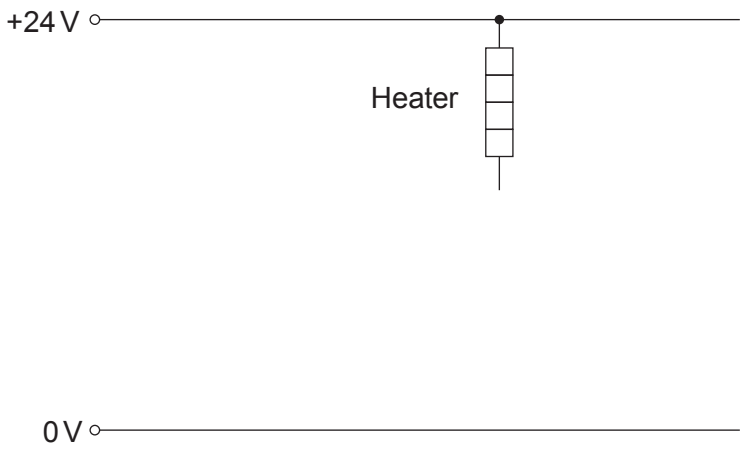
(b) (i) Complete the circuit diagram for a thyristor heater control, triggered by a push-switch S_1 and a resistor. [2]



(ii) The table shows data for the thyristor used in the heater control circuit.

Parameter	Value
Peak gate current	2 A
Minimum gate current	5 mA
Peak gate voltage	5 V
Minimum gate voltage	0.8 V
Holding current	12 mA
Maximum forward leakage current	0.5 mA

Use the data to calculate the maximum resistance of the resistor. [2]

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(iii) What is the minimum heater current needed to keep this thyristor in conduction, once triggered? [1]

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(iv) Modify the circuit diagram above to show how a second switch and additional components can be used to allow the heater to be switched off using capacitor commutation. [3]

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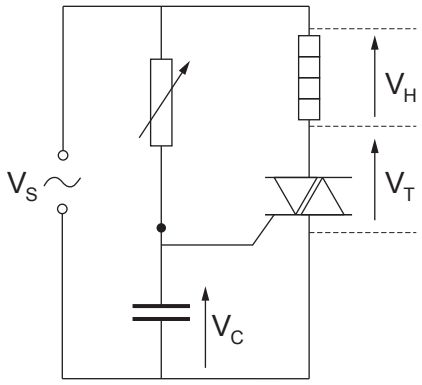
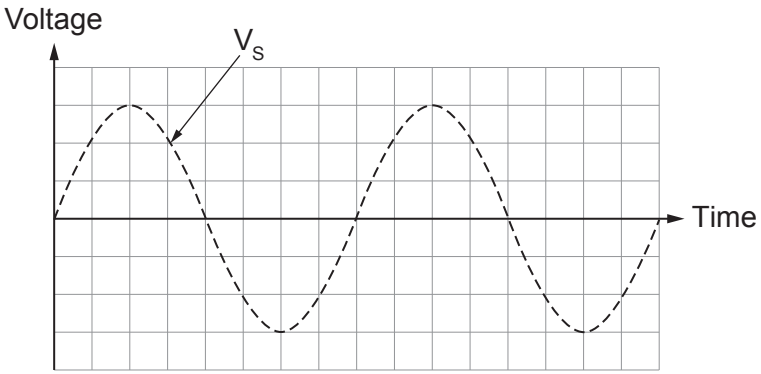
(c) A triac can use phase control to adjust the heat output of a heater.



(i) The variable resistor is set to create a phase shift of 45° between V_C and V_S. The graph shows the 50 Hz AC supply waveform, V_S.
Add the waveform of V_C to show this phase shift. [3]



(ii) The circuit uses a 1 μF capacitor. What is the resistance of the variable resistor needed to create the 45° phase shift? [2]

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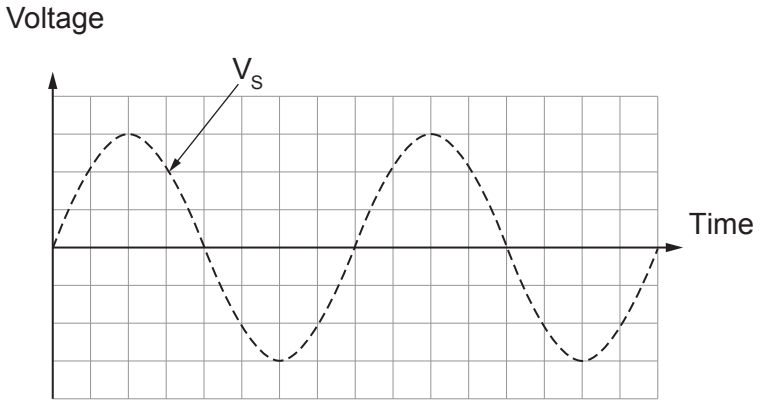
Examiner only

(iii) Draw the waveform of the voltage V_H across the heater. [3]



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