



GCE A LEVEL MARKING SCHEME

AUTUMN 2021

A LEVEL ELECTRONICS – COMPONENT 2 A490U20-1

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INTRODUCTION

This marking scheme was used by WJEC for the 2021 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

EDUQAS A LEVEL ELECTRONICS - COMPONENT 2

AUTUMN 2021 MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

cao = correct answer only

ecf = error carried forward

0	iactic		Marking datails		М	arks avai	lable	
Qu	iestic	DU		A01	AO2	AO3	Total	Maths
1.	(a)	(i)	Logic level $A = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1$	1	1		2	1
		(ii)	For X: Correct logic [1] Correct timing [1] For Q: Correct logic [1] Correct logic [1] Correct logic [1] Correct logic [1] Correct logic [1] Correct logic [1] For Q: Correct logic [1] Correct logic [1]	2	2		4	2
	(b)	(i)	YX = 11 [1]		1		1	1
		(ii)	Decimal = 3[1]Hex = 3[1]Allow ecf from binary answer to dec and hex answers.		2		2	2
		(iii)	Freq. at X = 1Hz[1][1]Freq. at Y = half of freq at X[1]Freq. at Z = freq at Y[1]	1	2		3	2
			Question 1 total	4	8	0	12	8

0	Question		Marking dataila		Marks available						
Q	uesuc	m	Marking details		AO1	AO2	AO3	Total	Maths		
2	(a)		$D_{C} = C (B + A)$ $D_{B} = \overline{B \oplus A}$ $D_{A} = C \overline{A}$	[1] [1] [1]		3		3	3		
	<i>(b)</i>		$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	[1] [1] [1]		3		3	3		
	(c)		Indicative content: State diagram:		2		4	6			

Questian	Marking details		М	arks avai	lable	
Question	Marking details	A01	AO2	AO3	Total	Maths
(C)	Indicative content:					
	 Count Down switch - meets the spec starts counting when closed. Always starts counting on '7' - does not meet the spec. It continues counting from its previous state, if the power supply is not disconnected, or from a random state on power up. Counts down from '7' to '0' - providing that it starts in the main sequence at '7', the count proceeds as a down count until it reaches the number '2' (010). Then it jumps to zero. It does not meet the spec. Stops counting when it reaches '0' - does not meet the spec. It reaches '000' but then enters a loop, alternating between '000' and '010'. 					
	 5-6 marks A detailed analysis of the system is given, including the state diagram. All factors identified above are evaluated accurately. There is a sustained line of reasoning which is coherent, relevant, substantiated and logically structured. 3-4 marks The analysis includes a correct state diagram. Most factors identified above are evaluated accurately. There is a line of reasoning which is partially coherent, largely relevant, supported by some evidence and with some structure.					

Question	Marking details		M	arks avai	lable	
Question		AO1	AO2	AO3	Total	Maths
	 1-2 marks The performance of the system is discussed in qualitative terms only. The main sequence of the state diagram is given and is correct. Two of the factors are evaluated correctly. There is a basic line of reasoning which is not coherent, largely irrelevant, supported by limited evidence and with very little structure. 0 marks No attempt made or no response worthy of credit.					
	Question 2 total	2	6	4	12	6

	Question	Marking dataila			Ма	arks avai	lable		
9	uesu	on			AO1	AO2	AO3	Total	Maths
3.	(a)	(i)	Time constant = RC = $100 \times 10^3 \times 2.2 \times 10^{-6} = 0.22s$	[1]		1		1	1
		(ii)	Time to charge to $4V = -RC \ln (1 - V_C/V_0)$ = -0.22 ln (1 - 4/6) = 0.24s Time to charge to $2V = -0.22 \ln (1 - 2/6) = 0.09s$ Time to charge from 2V to $4V = 0.24 - 0.09$ = 0.15s Use of formula or equivalent solution.	[1] [1] [1] [1] [1]	2	3		5	4
	(b)	(i)	Frequency ~ 4.5Hz	[1]		1		1	1
		(ii)	Voltage/V	[1] [1] [1] [1]	1	3		4	3
	(c)	(i)	Connections for pins 1, 3, 4 and 8 Timing network correct Buzzer correct $0.6 = 1.44 / (R_1 + 2 \times 10k) 10 \times 10^{-6}$ Use of formula Var. res. value = 220k Ω (Accept values in the range 220 to 250)	[1] [1] [1] [1] [1] kΩ)	2		3	5	3
			Question 3 total		5	8	3	16	12

	Question		Marking details					Ма	arks avai	lable	
ن	luesu	on		IVIč	arking details	-	AO1	AO2	AO3	Total	Maths
4.	(a)			● ^{Output} Two Abil Cor or e	o voltage dividers on inputs ity to adjust threshold rect orientation equivalent solution	[2] [1] [1]	1		3	4	
	(b)		sensor_check light buzz	clrf btfsc goto btfsc goto goto bsf goto bsf call goto	PORTB PORTA,0 light PORTA,1 buzz sensor_check PORTB,1 sensor_check PORTB,2 onesec sensor_check	[1] [1] [1] [1] [1] [1] [1] [1]	1	7		8	
	(c)	(i)	102 goto f 103 retfie	ire		[1] [1]	1	1		2	
		(ii)	Line 100 swit Line 101 test If pressed, the ISF If not pressed, the (or equivalent ans	tches on th ts the state R ends. siren cont wers)	e siren of the reset switch. inues to sound. on the siren	[1] [1]	1	1		2	
			Question 4 total				4	9	3	16	0

	Question		Marking dataila		Ма	arks avai	lable	
6	luesu	on	Marking details	A01	AO2	AO3	Total	Maths
5.	(a)	(i)	$\begin{array}{c} & \begin{array}{c} & \begin{array}{c} & Circuit\ correct & [1] \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ $			3	3	1
		(ii)	Voltage/V 6.0 4.0 0 utput o -2.0 -4.0 -4.0 -6.0 -4.0 -6.0 -7 me Correct amplitude (5V) [1] Correct phase [1]	1	1		2	1
		(iii)	Bandwidth = $10 \times 10^6 / 100 = 10^5$ [1]Audio frequency range = 20 kHz so much smaller.[1](or equivalent)[1]	1	1		2	1
	(b)	(i)	Voltage/V Switch X open 2.0 Switch Y closed 0 -2.5V -4.0 time Correct shape [1] Correct voltage (-2.5V) [1]	1	1		2	1
		(ii)	Voltage/V 6.0 Switch X closed 4.0 Switch Y closed 2.0 -2.5V -2.0 -6.0 -8.0 -2.5V -2.0 -2.5V -2.5V -2	1	2		3	2

0	Question		Marking details	Marks available						
Q	uesu				AO2	AO3	Total	Maths		
	(c)	(i)	15Ve Collectors to power rails [1] Common base to op-amp output [1] Common emitter to L/S [1] Op-amp inputs correct [1] Negative feedback correct [1]	3	2		5			
		(ii)	Optimum output impedance = 8Ω [1]	1			1			
			Question 5 total	8	7	3	18	6		

	Question		Marking details		Marks available						
<u> </u>	luesu	on			AO1	AO2	AO3	Total	Maths		
6.	(a)		Audio frequency range is 20Hz to 20kHz. Sampling frequency is more than twice highest audio freq. (or equivalent)	[1]	1			1			
	<i>(b)</i>		Bit rate = no. of samples per second x no. of bits per sample = $50,000 \times 12 = 600$ kbps File size = bit rate x duration of sampling = $600,000 \times 20 \times 60 = 720$ Mb Use of formulae	[1] [1] [1]	1	2		3	2		
			Question 6 total		2	2	0	4	2		

	Juooti	o.n	Morking dotailo			M	arks avai	lable	
	luesu	on			A01	AO2	AO3	Total	Maths
7.	(a)		No negative voltage Half-wave signal	[1] [1]	1	1		2	1
	(b)	(i)	Correct connections Vout Polarity correct	[1] [1]		2		2	
		(ii)	Ripple voltage = I / f x C = 1.8V (Accept 1.82V) Use of formula Correct answer	[1] [1]	1	1		2	2
		(iii)	Voltage/V 40 20 -20 -20 -40 Voltage/V time Evidence of ripple Accurate level of ripple (Accept initial growth from 0V)	[1] [1]		2		2	2
		(iv)	Modify circuit to full-wave rectifier Increase value of capacitance	[1] [1]	2			2	

Question	Marking details		Ма	arks avai	lable	
Question		AO1	AO2	AO3	Total	Maths
(c) (i)	Using P=IxV, I = P/V = 500/8.2 = 61mA[1]Use of re-arranged formula[1]Answer with correct multiplier[1]	1	1		2	2
(ii)	Using V = IxR, R = V/I = $(15-8.2) / 61 \times 10^{-3} = 110\Omega$ [1]Use of re-arranged formula[1]Evidence of voltage drop calculation across R[1]Answer[1]	1	2		3	3
(iii)	Maximum output current = $61-5=56$ mA[1]Output voltage = 8.2 V[1]Using V = IxR, R = V/I = $8.2/56 \times 10^{-3} = 146\Omega$ [1]	1	2		3	3
(d) (i)	All connections correct [1]	1			1	
(ii)	New Zener voltage = VOUT + Voltage drop across transistor = $8.2 + 0.7$ [1] = $8.9 \vee$ [1]	1	1		2	
(iii)	Resistor Zener circuit only regulating transistor instead of load, lower power required.	1			1	
	Question 7 total	9	13	0	22	16

	Juanti	on	Marking dataila			Ма	arks avai	lable	
	Luesu	on			AO1	AO2	AO3	Total	Maths
8.	(a)	(i)	Thyristor conducts in ony one direction. A triac can conduct in both. (or equivalent)	[1]	1			1	
		(ii)	Forward bias Sufficient gate current (or equivalent)	[1] [1]	2			2	
	(b)	(i)	Rapid turn-on. (or equivalent)	[1]	1			1	
		(ii)	Increasing resistance reduces brightness of the lamp. (or equivalent) It increases the phase shift between V_c and V_s OR It delays the turn-on each half-cycle	[1] [1]	1	1		2	
	(c)	(i)	12 squares = 1 cycle = 1/50s = 20ms Triac is 'on' for 8 squares each cycle = 13.3ms (or equivalent)	[1] [1]		2		2	2
		(ii)	Forward breakover voltage = 40V	[1]		1		1	
		(iii)	V_c lags by one square = 1/12th of a cycle 1 cycle = 360° , hence phase difference = 30° lag	[1] [1]		2		2	2

Question		Marking details	Marks available						
6	uestion	Warking details	AO1	AO2	AO3	Total	Maths		
	(iv)	$\begin{array}{l} {\sf R} = {\sf X}_{\sf C} \tan \phi \\ {\sf X}_{\sf C} \!$	1	2		3	2		
		Question 8 total	6	8	0	14	6		

Question		<u></u>	Marking dataila		Marks available				
				AO1	AO2	AO3	Total	Maths	
9.	(a)		→ Low-pass → Sampling → ADC → PISO register → ADC → PISO Sampling gate and clock [1] ADC [1] PISO PISO register and clock [1] PISO register and clock [1]	3			3		
	(b)	(i)		1	2		3	2	
		(ii)	Voltage gain 100 100 1000 1000 10000 Frequency/Hz Correct low freq. gain 20 [1] Correct break freq. 4.4kHz [1] Correct shape [1] (Allow e.c.f. from (i)	1	2		3	2	
	(c)		The staircase waveform is passed through a low pass filter, which 'smoothes out' quantisation steps. (or equivalent.) [1]	1			1		
	(d)	(i)	Output saturates at +10V/-10V[1]Switching thresholds are +8V/-2V[1]		2		2	2	

Question		0.12	Marking dataila			Marks available					
9	Question			AO1	AO2	AO3	Total	Maths			
		(ii)	Circuit diagram correct In positive sat: (10 - 2) / $R_2 = (2 - 2) / R_1$ In negative sat: (8 - 2) / $R_1 = (2 - 10) / R_2$ Calculation of resistor ratio $R_2 = 2 \times R_1$ Resistors > 1k Ω	[1] [1] [1] [1]			4	4	3		
	(e)	(i)	One sample occurs every $1/12000s$. In this time, SIPO clock processes the 10 bits in the sample. Maximum SIPO period is $1/12000 \times 10 s$ Minimum SIPO frequency = $12000 \times 10 = 120$ kHz.		1	1		2	2		
		(ii)	10 bits creates 2^{10} voltage levels separated by 3mV. Biggest output is $(2^{10}-1)x3mV = 3.07V$. (Accept 3.1V) (or equivalent approach)			2		2	2		
			Question 9 total	7	9	4	20	13			

Question		• •	Marking details					Marks available					
		on						AO1	AO2	AO3	Total	Maths	
10	(a)		Does not transmit e/m radiation[1]Difficult to tap without affecting the whole transmission[1](or equivalent)[1]					2			2		
	(b)		Property	LED	LD			2			2		
			Cost	Low	High	LED correct LD correct							
			Power output	Low	High		[1] [1]						
			Speed	Low	High		[,]						
			Frequency range	High	Low								
	(c)		Less attenuation than for visible light[1]so fewer repeaters needed.[1]					2			2		
			Question 10 total					6	0	0	6	0	

A LEVEL ELECTRONICS - COMPONENT 2

Question	A01	AO2	AO3	TOTAL MARK	MATHS	
1	4	8	0	12	8	
2	2	6	4	12	6	
3	5	8	3	16	12	
4	4	9	3	16	0	
5	8	7	3	18	6	
6	2	2	0	4	2	
7	9	13	0	22	16	
8	6	8	0	14	6	
9	7	9	4	20	13	
10	6	0	0	6	0	
TOTAL	53	70	17	140	69	

SUMMARY OF MARKS ALLOCATED TO ASSESSMENT OBJECTIVES

A490U20-1 EDUQAS GCE A Level Electronics – Component 2 MS A21/DM