Surname	Centre Number	Candidate Number
First name(s)		2

GCE A LEVEL

O21-A490U20-1

A490U20-1

TUESDAY, 12 OCTOBER 2021 – MORNING

ELECTRONICS – A level component 2
Application of Electronics

2 hours 45 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**12**	
2.	**12**	
3.	**16**	
4.	**16**	
5.	**18**	
6.	**4**	
7.	**22**	
8.	**14**	
9.	**20**	
10.	**6**	
Total	**140**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen. Do not use gel pen or correction fluid.

You may use a pencil for graphs and diagrams only.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet. If you run out of space, use the additional page(s) at the back of the booklet, taking care to number the question(s) correctly.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in question **2***(c)*.

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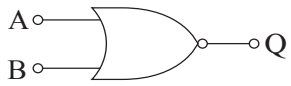
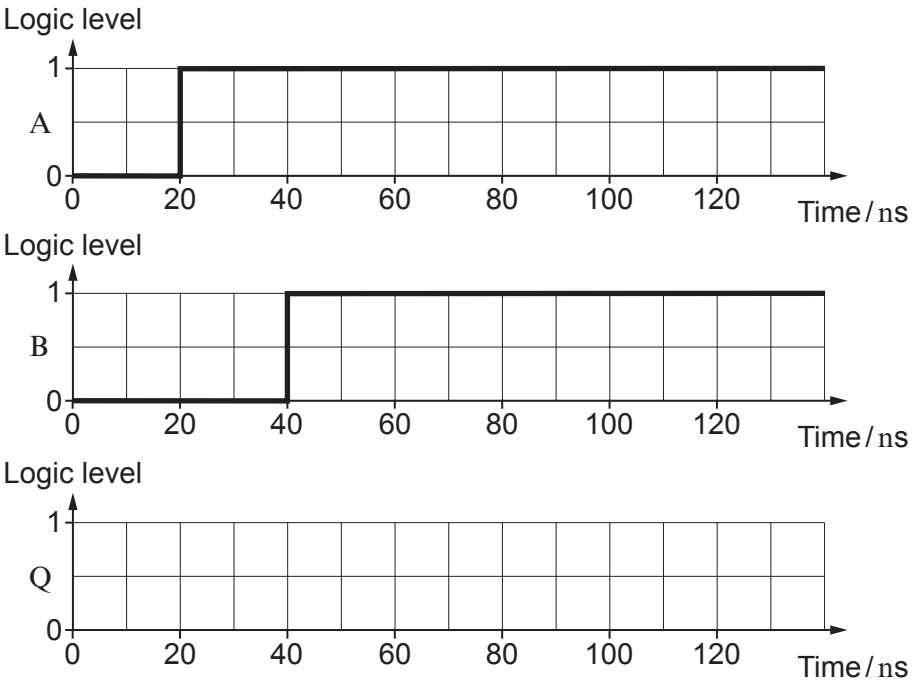
Answer **all** *questions.*

1. *(a)* The 2-input NOR gate shown in the diagram has a propagation delay of 60 ns.



(i) Complete the timing diagram for the Q output. Assume that the inputs have been low (0) for a long time. [2]



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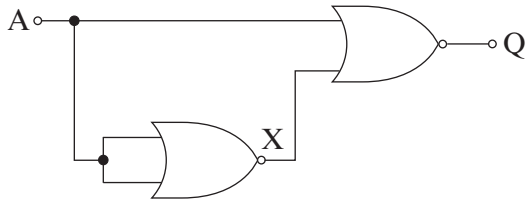
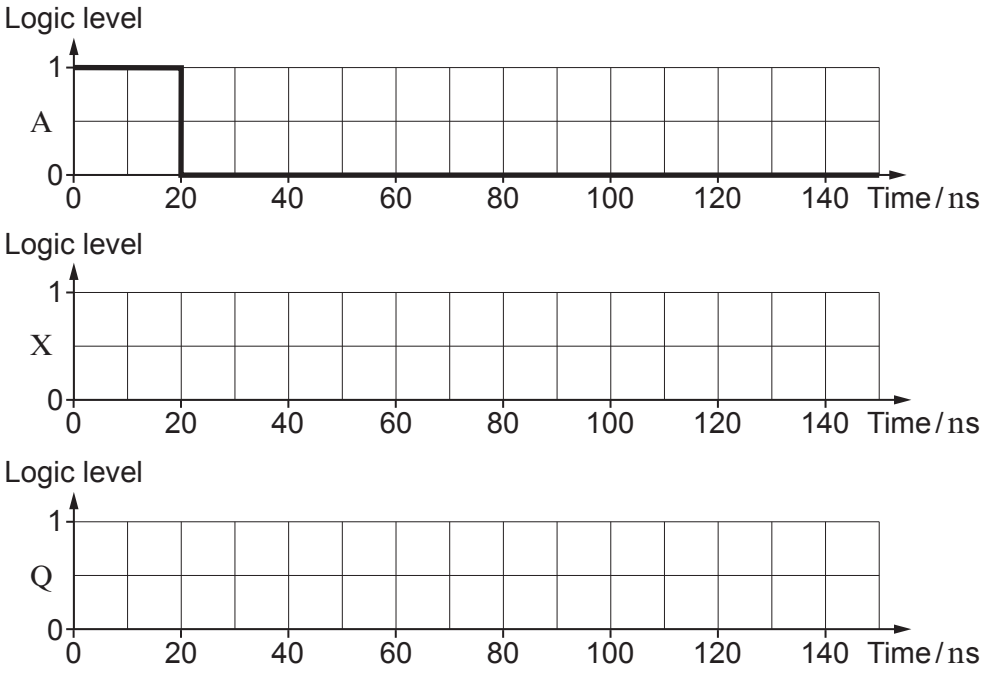
(ii) Two of these NOR gates are connected as shown in the following diagram:



The signal shown in the graph below is applied to input A. Assume that the input A has been high (1) for a long time.

Use the axes provided to show the resulting signals generated at X and Q. [4]



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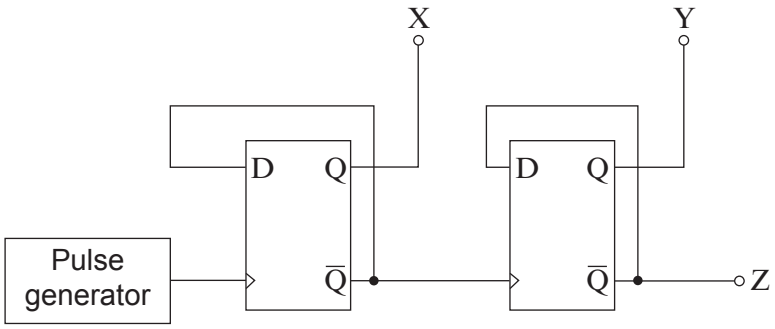
(b) Two rising-edge D-type flip-flops are connected as shown in the following circuit diagram.



(i) Initially, both D-types are reset.

What is the binary output YX after three clock pulses? [1]

.....

(ii) Convert this answer to: [2]

- a decimal number; .....
- a hexadecimal number. .....

(iii) The pulse generator has a frequency of 2 Hz. [3]

What is the frequency of the signal at:

- output X .....
- output Y .....
- output Z .....

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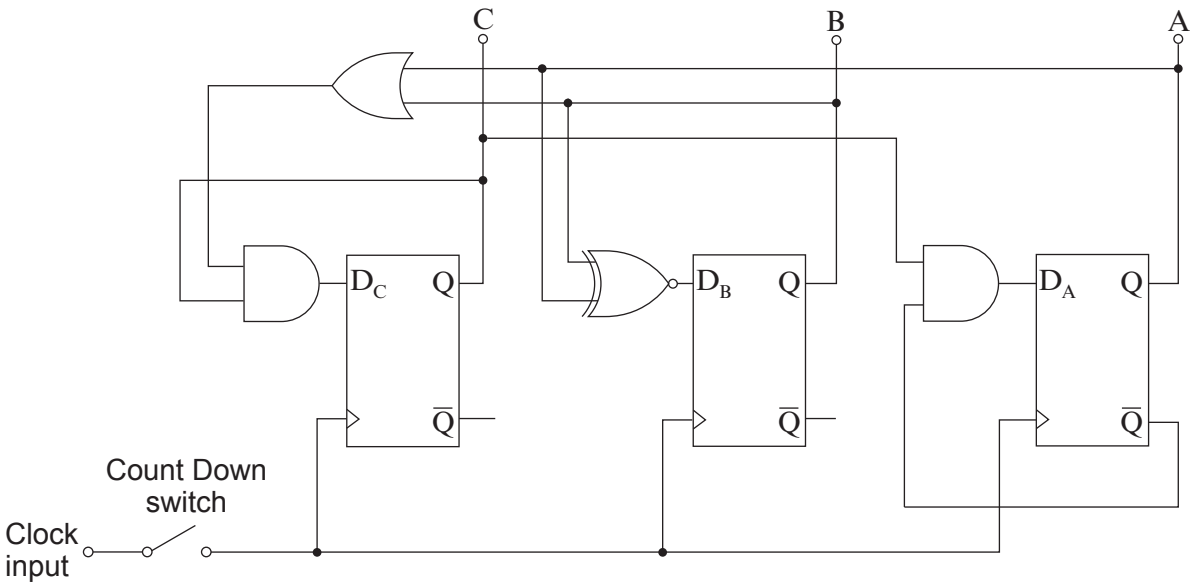
2. The diagram below shows a suggested circuit for a down counter.

(a) Complete the Boolean equations for D_C, D_B and D_A in terms of outputs C, B and A for the following system. [3]



D_C = ...

D_B = ...

D_A = ...

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(b) Complete the table for the system to show the signals present at the inputs of the D-type flip-flops for each value of the outputs C, B and A. [3]

C	B	A	D_C	D_B	D_A
1	1	1			
1	1	0			
1	0	1			
1	0	0			
0	1	1			
0	1	0			
0	0	1			
0	0	0			

(c) A student has the following specification for the system:

The counter must:

- start counting down when the 'Count Down' switch is closed;
- always start counting on the number '7' (111_2);
- then count down from '7' to '0';
- stop counting when it reaches '0'.

Evaluate the suggested circuit as a solution that meets this specification.

Your evaluation should include the state diagram for the system. [6 QER]

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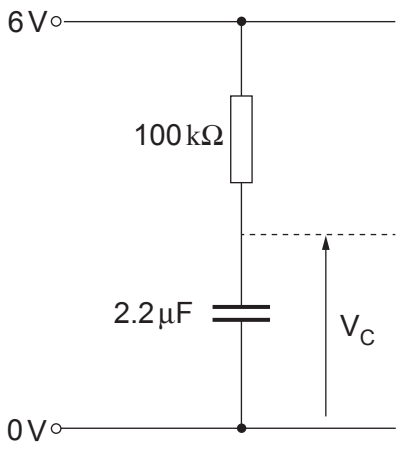
3. *(a)* The circuit diagram shows a RC network.



Calculate:

(i) the time constant for the network; [1]

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(ii) the time taken for V_C to change from 2 V to 4 V. [5]

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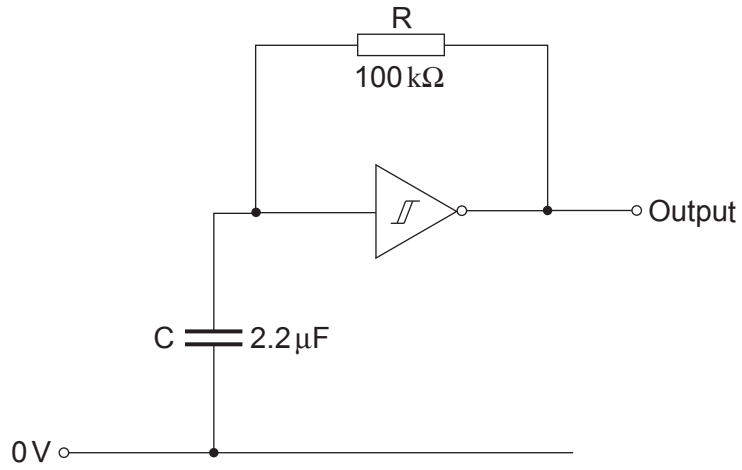
(b) A Schmitt inverter astable has thresholds of 2 V and 4 V and its output saturates at 6 V and 0 V.



(i) Estimate the frequency of the astable. [1]

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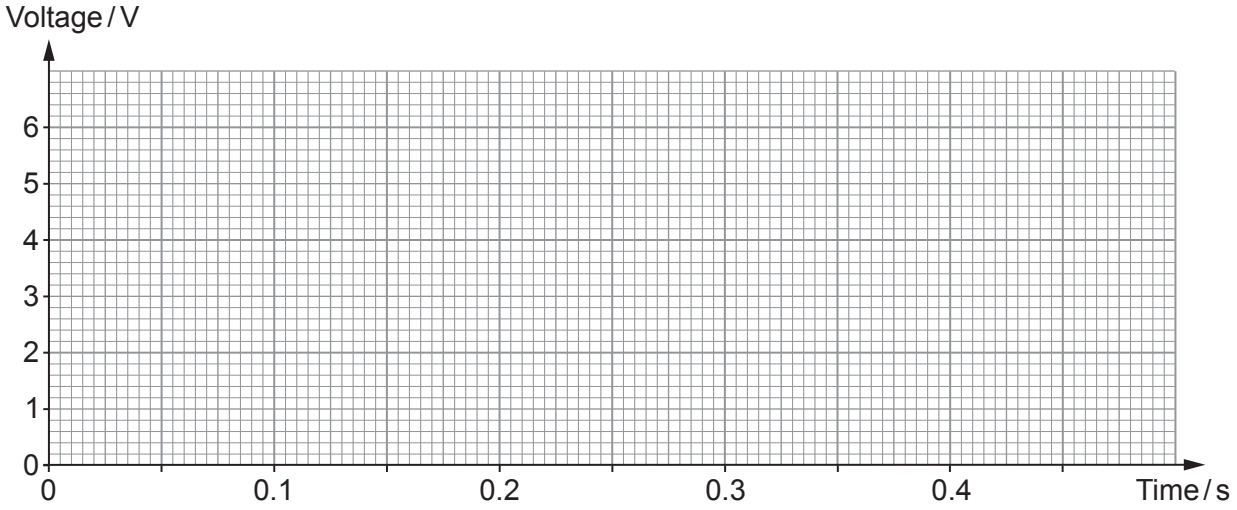
(ii) Draw two graphs on the axes below to show how the voltages at the input and output of the Schmitt inverter change over time when the astable has been pulsing for some time. [4]



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(c) A 555 astable circuit is used to drive a buzzer.

The circuit has a frequency which can be varied down to 0.6 Hz.
It includes a 10 μF capacitor and a 10 kΩ fixed resistor in the timing network.

Design the 555 astable circuit. Complete the following circuit diagram with your design, labelling all significant component values. [5]

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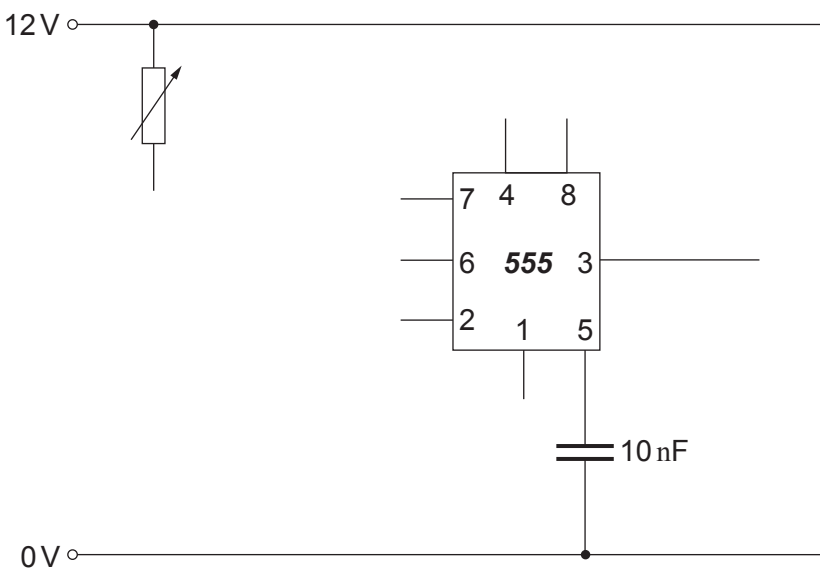

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4. *(a)* A light-sensing sub-system is used as part of a bank security system.
The sub-system senses the ambient light level outside the building and its output switches high when it gets dark.

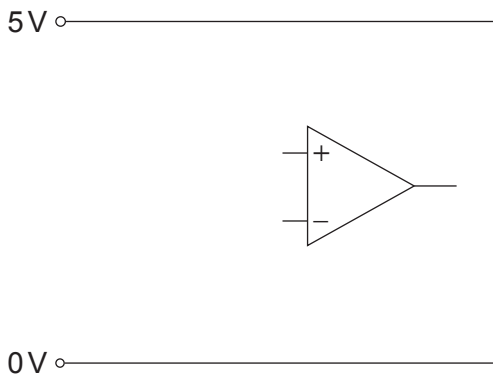
The sub-system includes:

- a light-dependent resistor (LDR);
- a comparator.

It must be possible to adjust the light level at which the output goes high.

Design a suitable light-sensor sub-system.

Complete the circuit diagram to show your design. [4]



(b) A 16F88 PIC microcontroller is used in the security system in a bank.

- When it gets dark, the microcontroller turns on the lights outside the bank.
- When the bank door opens, a buzzer sounds, briefly, behind the counter.
- The microcontroller also detects fires in the building. When a fire occurs, a siren is activated until a reset switch is pressed.

The system uses:

- the light-sensing sub-system from part *(a)*;
- a microswitch sub-system to detect when the bank door opens. It outputs a logic 1 signal when the door is opened.

Peripheral devices are connected to the microcontroller as follows:

- The light-sensor sub-system is connected to PORT A bit 0.
- The microswitch sub-system is connected to PORT A bit 1.
- The outside lights are activated when PORT B bit 1 is set.
- The buzzer is activated when PORT B bit 2 is set.

Examiner only

Part of the main program is given below.
It uses a subroutine called '*onesec*' to create a one second delay.

Complete the unfinished instructions. [8]

```
sensor_check    clrf    .....       ; switch off all output devices
                btfsc   PORTA,0     ; check the ambient light-sensor
                goto    .....       ; switch on outside lights
door_check      .....   PORTA,1     ; check the door sensor
                goto    buzz        ;
                .....   sensor_check ; check the state of the sensors again
light           bsf     .....       ; switch on the outside lights
                goto    door_check  ;
buzz            .....   PORTB,2     ; switch on the buzzer for
                .....   onesec      ; one second
                goto    .....       ; check the state of the sensors again
```

(c) The security system also incorporates a fire detector.
This uses a temperature-sensing sub-system to trigger an interrupt, which switches on a siren.

The sub-system contains:

- a siren, activated when PORT B bit 3 is set;
- a reset switch, connected to PORT A bit 2, to reset the siren.

(i) Part of the interrupt service routine (ISR) is listed below:

```
100   fire    bsf     PORTB,3
101           btfss   PORTA,2
102           goto    .....
103           bcf     PORTB,3
104           .....                 ; return from interrupt
```

Complete the unfinished instructions in lines 102 and 104. [2]

(ii) Describe the effect of lines 100 and 101. [2]

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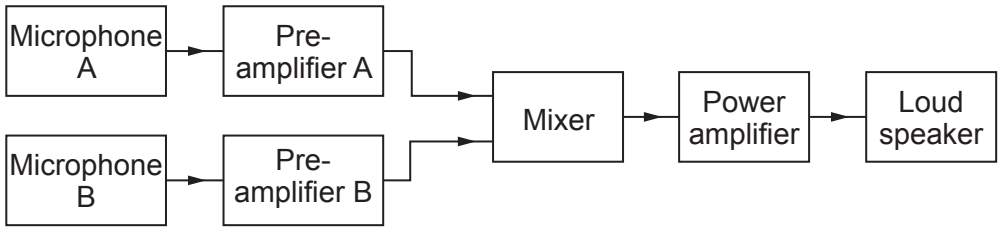
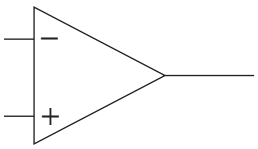
5. The signals from two microphones are combined using the system shown in the block diagram below.



The circuit is powered from a ± 15 V supply.

(a) (i) Each preamplifier is based on an op-amp having a gain-bandwidth product of 10 MHz. Preamplifier A has a voltage gain of 100.

Design a single-stage voltage amplifier for this preamplifier. [3]



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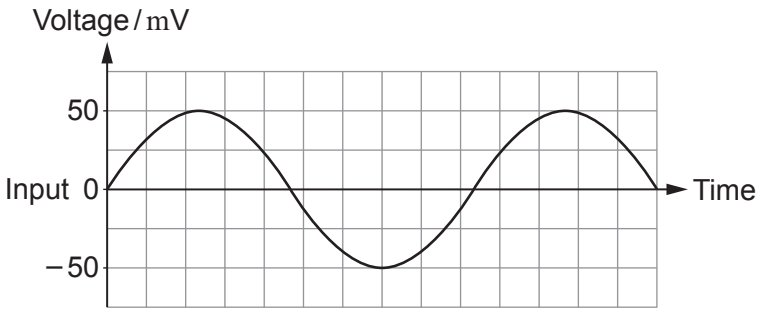
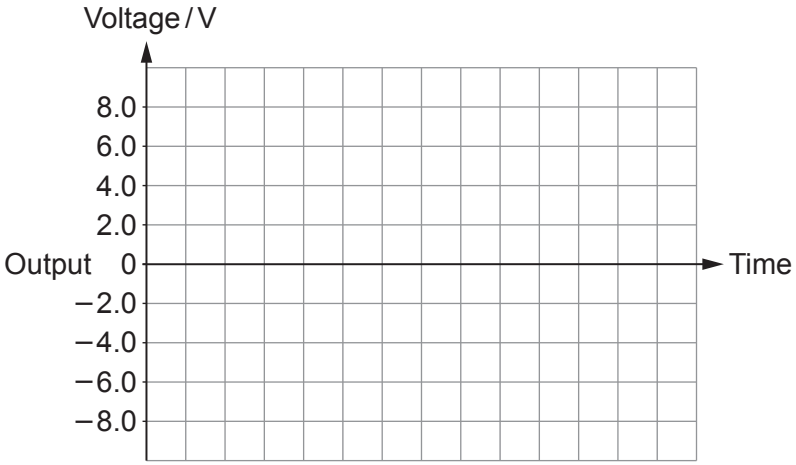
(ii) The signal shown in the top graph is applied to the input of preamplifier A. Use the axes provided to draw the corresponding signal produced at the output of the preamplifier. [2]





(iii) Explain why this preamplifier is suitable for the full audio frequency range. [2]

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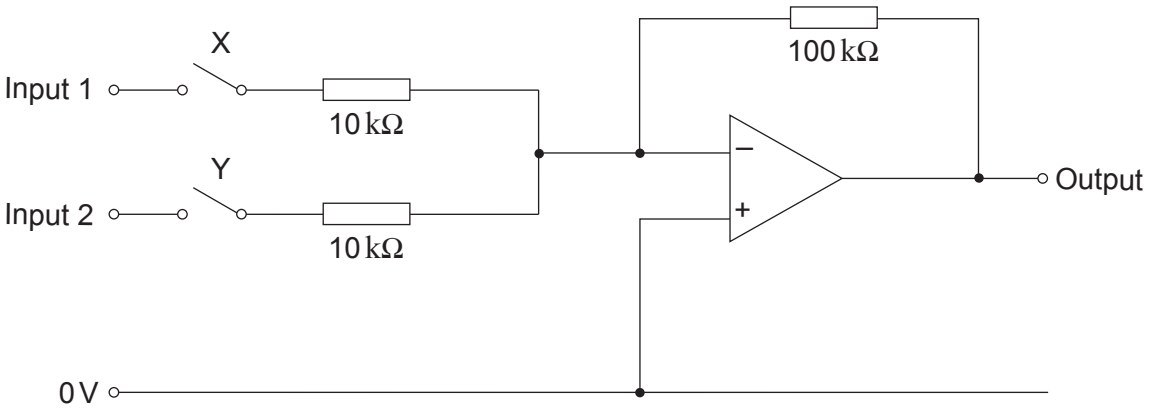
(b) The circuit diagram for the mixer is shown below.



It is tested by applying a sine wave with an amplitude of 0.5 V to input 1 and a steady DC voltage of +0.25 V to input 2. These are shown in the upper two graphs.

Use the axes provided opposite to draw the mixer output signal when:

(i) switch X is open and switch Y closed; [2]

(ii) both switches are closed. [3]

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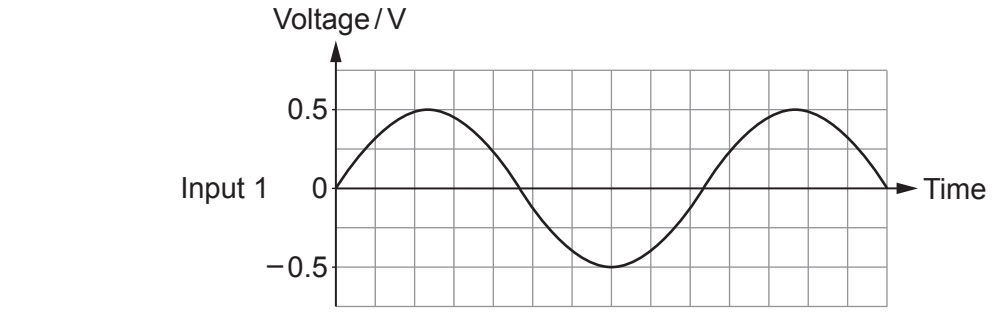

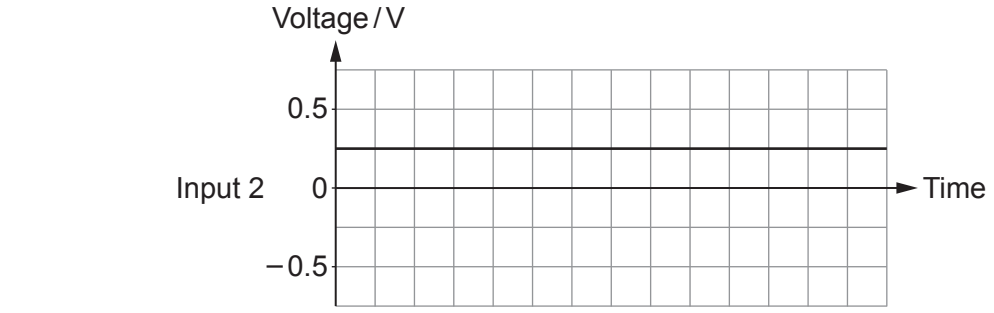

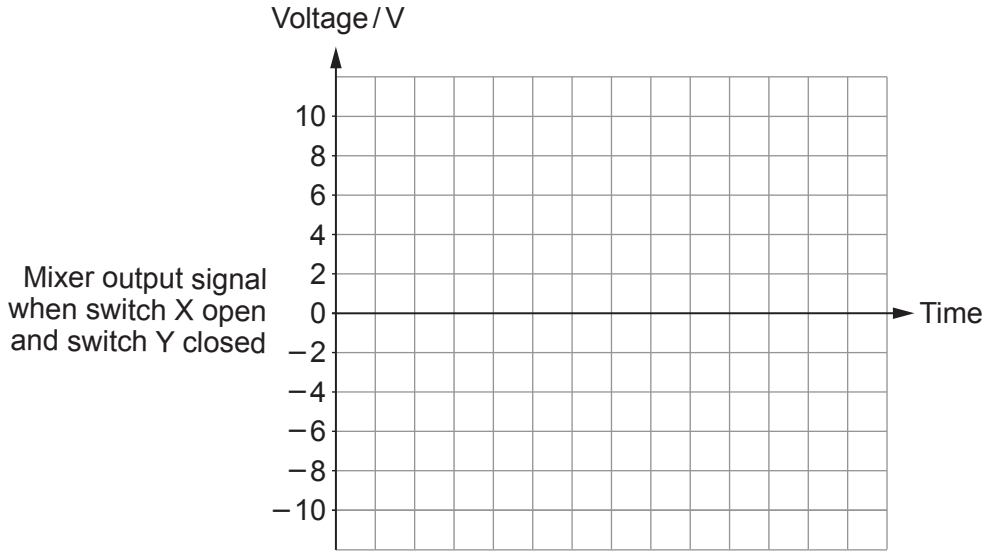

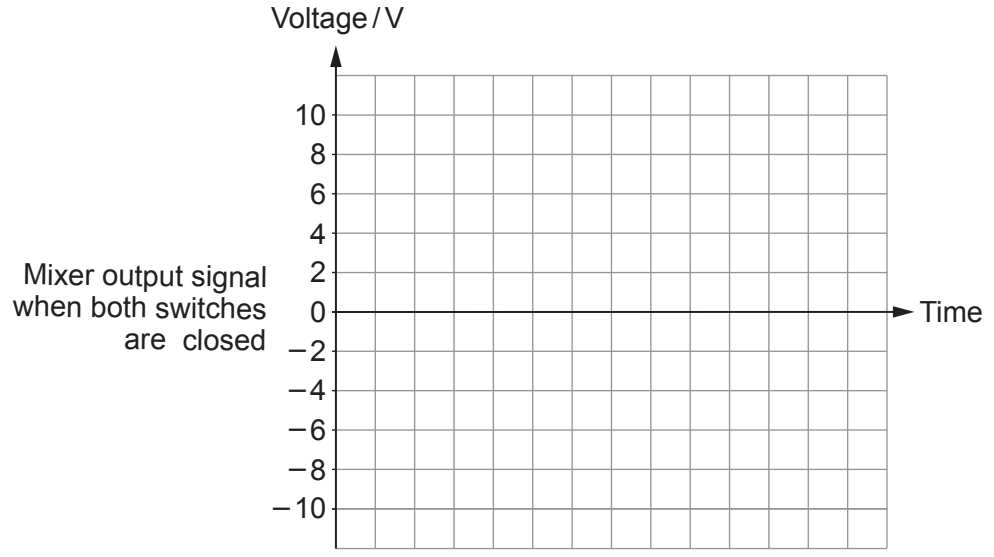

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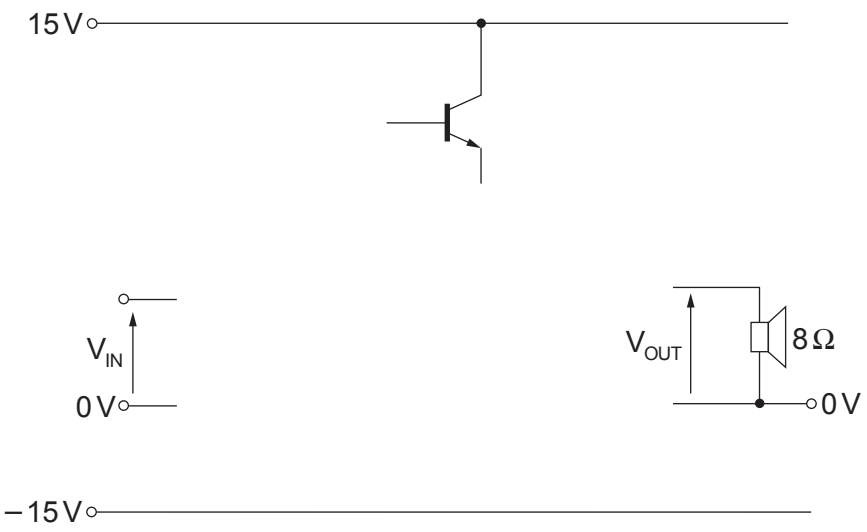
(c) The next diagram shows the incomplete circuit for the push-pull power amplifier.



(i) Complete the circuit diagram, including an op-amp voltage follower to correct crossover distortion. [5]

(ii) What value of output impedance for the power amplifier would maximise the power transferred from the power amplifier to the loudspeaker? [1]

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6. A recording studio makes digital recordings using a sampling frequency of 50 kHz.
Each sample contains 12 data bits.

(a) Explain why this sampling frequency is suitable for audio recording. [1]

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(b) A recording lasts 20 minutes.
Calculate the bit-rate (in kbps) and the file size of the resulting digitized signal. [3]

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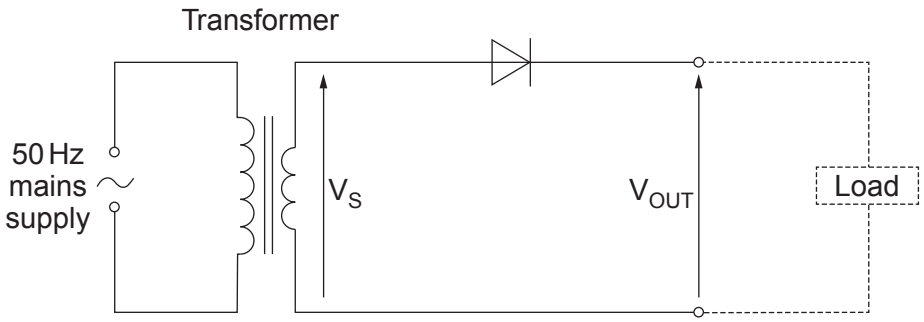
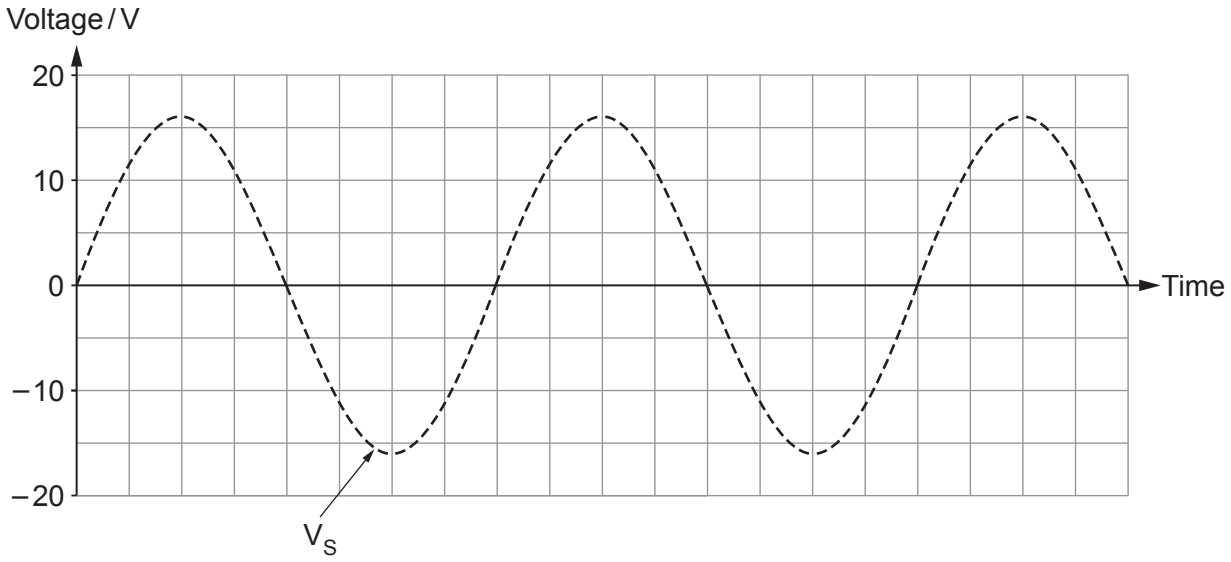
7. The following circuit diagram shows a half-wave rectified power supply connected to a load.



(a) On the axes provided below, draw a graph of the output voltage V_{OUT}. [2]

The voltage, V_S, across the transformer secondary, is shown as a dashed line.



(b) (i) Add a labelled 2200 μF polarised capacitor to the circuit diagram above to smooth the output. [2]

(ii) Calculate the size of the ripple voltage produced when the load current is 0.2 A. [2]

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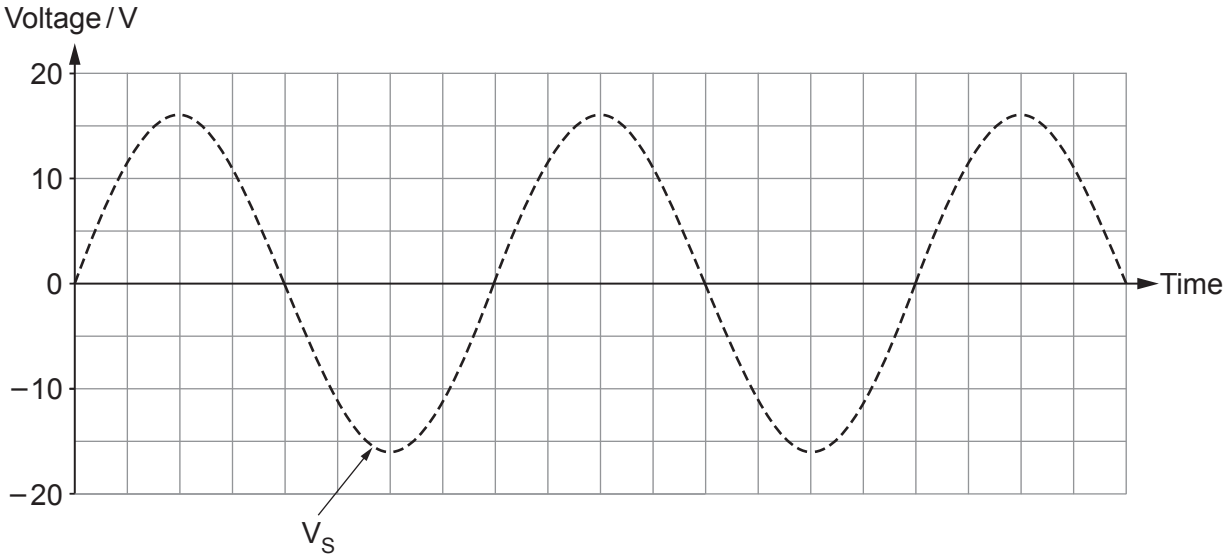
(iii) On the axes provided below, draw a graph of the new output voltage V_{OUT}. [2]



(iv) Describe **two** modifications to the power supply that would reduce the ripple voltage for this value of load current. [2]

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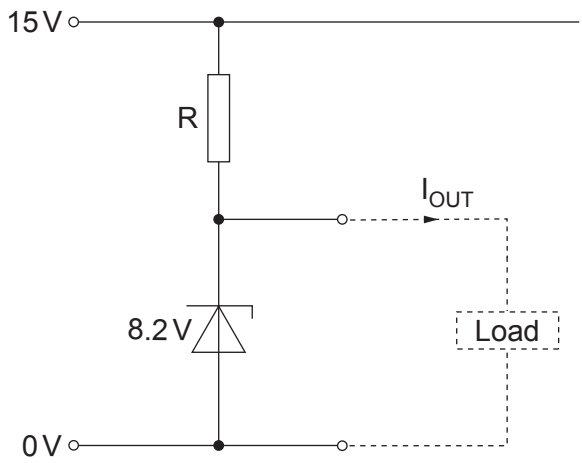
(c) The power supply is modified by adding a zener voltage regulator sub-system, using a 8.2 V, 500 mW zener diode.

It is tested in the circuit shown below. The zener diode stays in reverse breakdown provided that the holding current through it does not drop below 5 mA.



(i) What is the maximum current that can flow through the zener diode without exceeding its power rating? [2]

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(ii) Calculate the resistance of resistor R which allows this maximum current to flow through the zener diode. [3]

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(iii) Calculate the lowest value of load resistance that can be used whilst maintaining the output voltage. [3]

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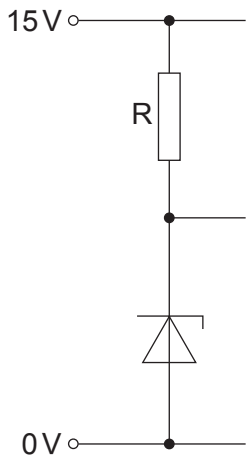
(d) The voltage regulator sub-system is modified by adding a transistor, connected as an emitter follower.

(i) Complete the following circuit diagram to show this modification. [1]



(ii) To maintain the output of 8.2 V, what is the new zener voltage required? [2]

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(iii) Explain why a different value of resistance would be used for resistor R. [1]

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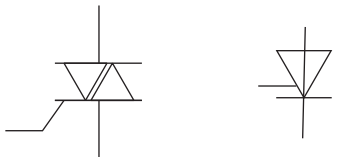
8. *(a)* Here are the circuit symbols for a triac and a thyristor.



(i) How does the behaviour of a triac differ from that of a thyristor? [1]

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(ii) State **two** conditions required to trigger a thyristor into conduction. [2]

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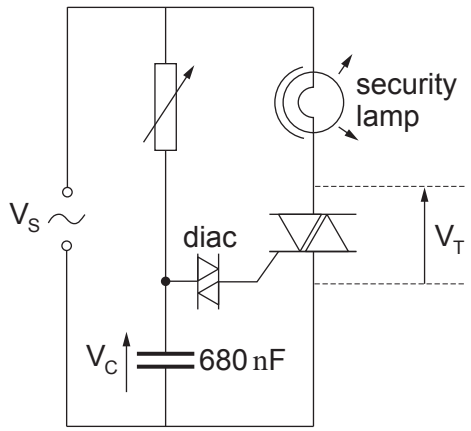
(b) The circuit diagram shows a triac used to control a security lamp using phase control.



(i) Explain how the diac reduces heat dissipation in the triac. [1]

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(ii) What is the effect on the lamp of **increasing** the resistance of the variable resistor? Explain why this happens. [2]

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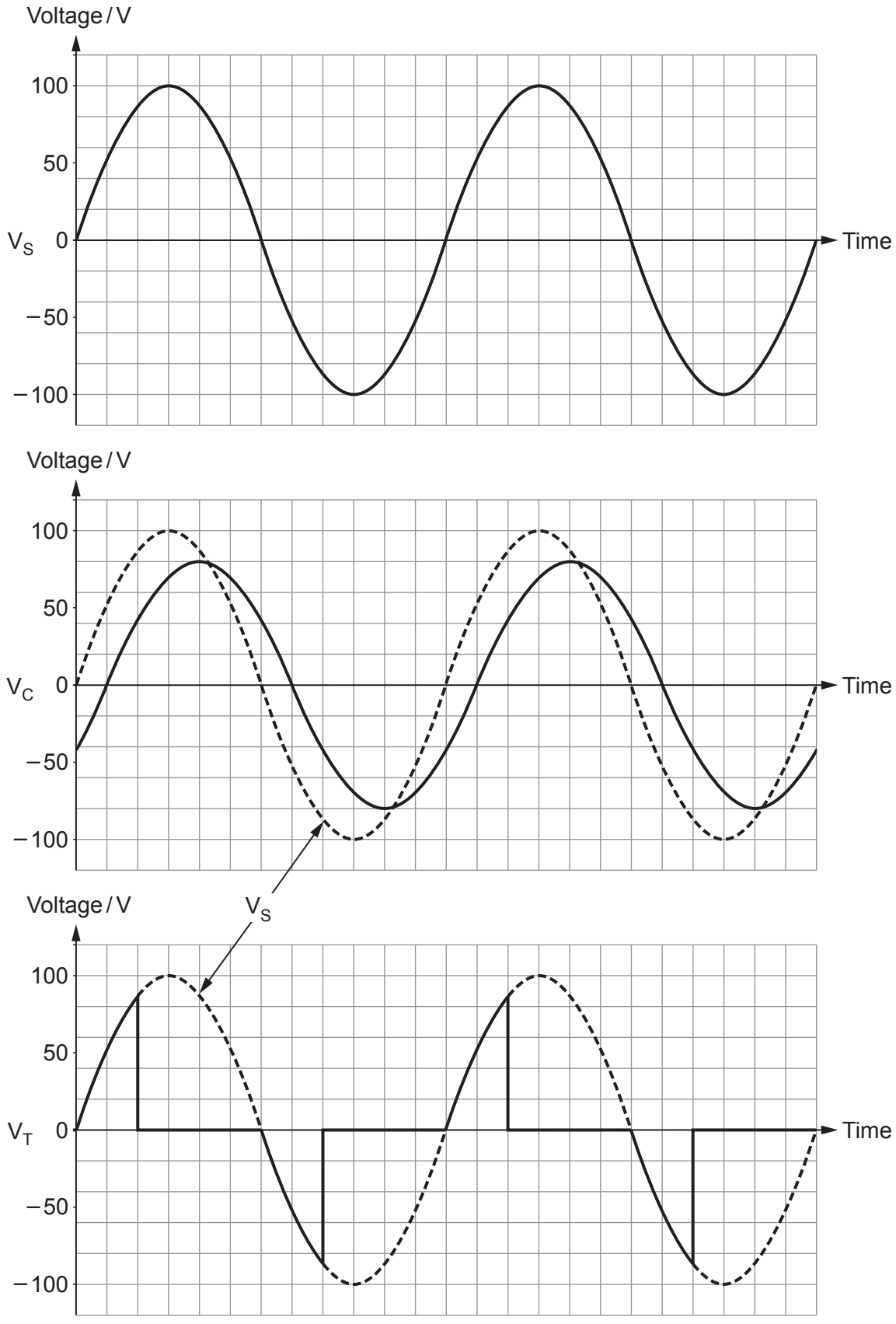
(c) The graphs below show some of the signals present in this circuit.



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Use the information in the graphs to answer the following questions:

(i) The AC frequency is 50 Hz.
For how long in each cycle of the mains supply is the triac switched on? [2]

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(ii) What is the breakover voltage of the diac? [1]

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(iii) Estimate the phase shift between V_C and V_S, and show how you arrive at your answer. [2]

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(iv) What value of the variable resistor would achieve a phase shift of 45°? [3]

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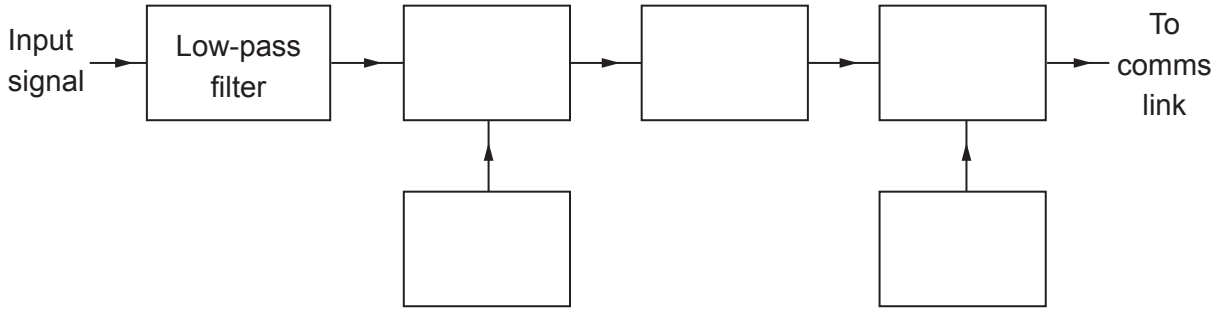
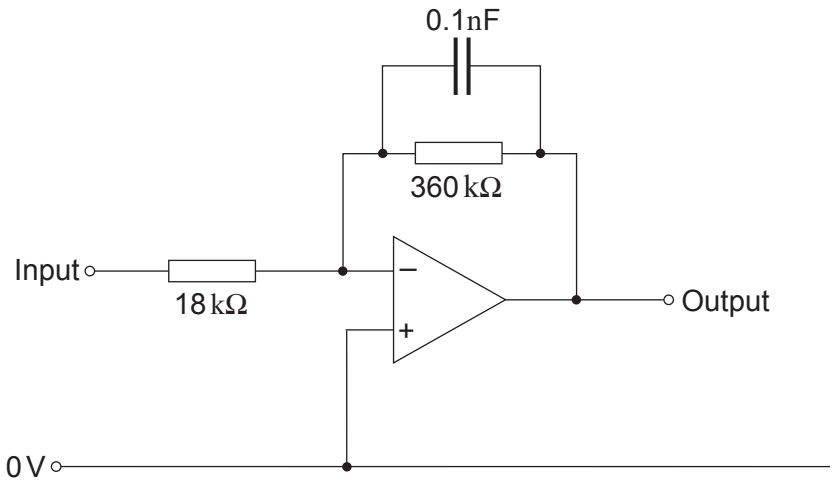
9. *(a)* Complete the block diagram for a PCM transmitter. [3]



(b) The circuit diagram below shows a low-pass active filter.



(i) Calculate the break frequency for this filter. [3]

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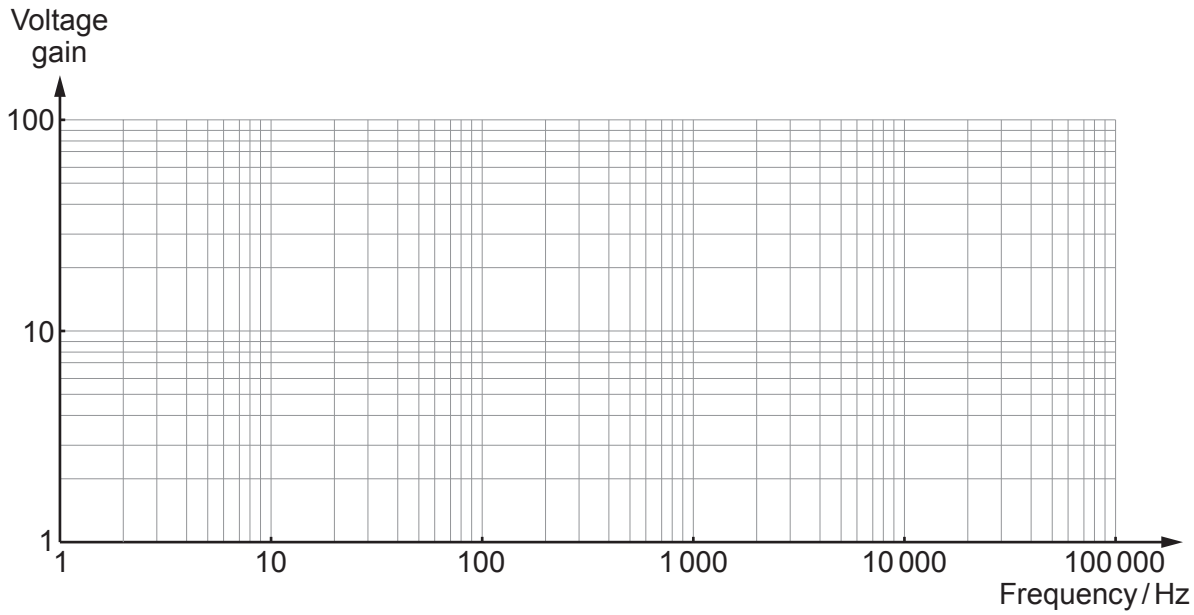
Examiner only

(ii) Use the log/log axes below to show the frequency response of this filter. [3]



(c) In a PCM **receiver**, what is the function of the low-pass filter? [1]

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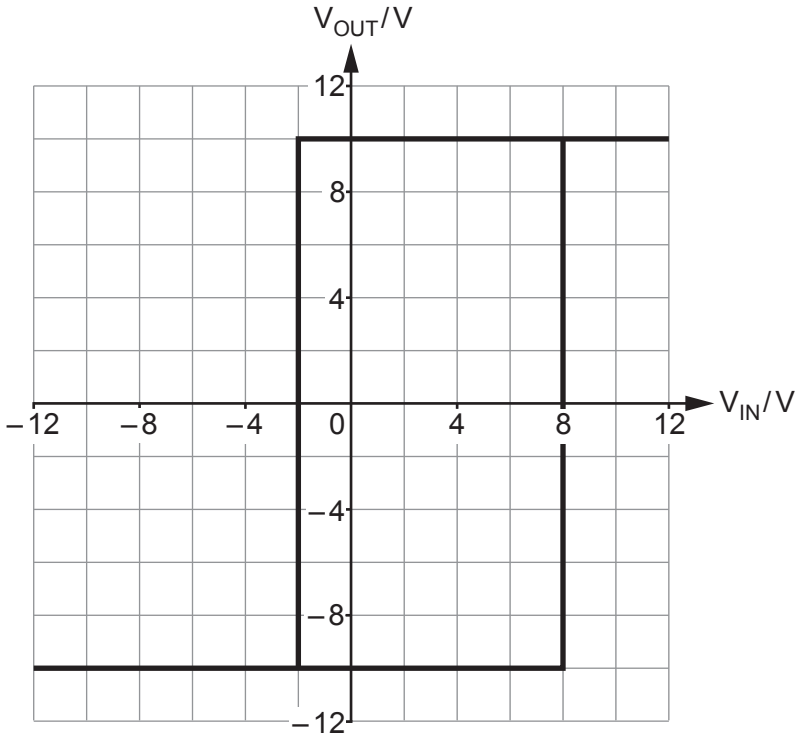
(d) The PCM receiver also contains a Schmitt trigger. Its characteristics are shown in the following graph:

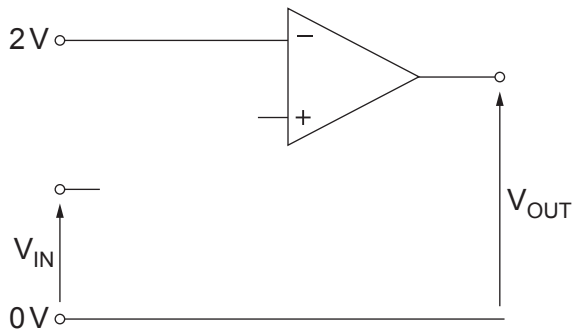


(i) For this Schmitt trigger, write down: [2]

- the saturation voltages .....
- the switching thresholds. .....

Examiner only

(ii) The incomplete circuit diagram for the Schmitt trigger is shown below, using a 2 V reference voltage.
Design a suitable circuit for the Schmitt trigger and complete the diagram to show your design, labelling all resistors with suitable values. [4]



(e) The PCM receiver uses a 10-bit DAC, having a step size of 3 mV to convert the digital signals it receives into analogue format.

The PCM system uses a sampling frequency of 12 kHz.

(i) What is the minimum frequency that can be used for the SIPO clock in the receiver? [2]

(ii) What is the maximum voltage possible at the output of the DAC? [2]

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10. *(a)* Explain why communications sent over an optical fibre link are more secure than those sent over radio or copper wire media links. [2]

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(b) Compare the properties of LEDs and laser diodes by completing the following table, adding the words 'lower' or 'higher' in each box. [2]

Property	LED	Laser diode
Cost		
Power output		
Speed		
Frequency range emitted		

(c) Why is infra-red preferred to visible light in optical fibre communication? [2]

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