Surname	Centre Number	Candidate Number
First name(s)		2

GCE AS

B490U10-1

Z22-B490U10-1

TUESDAY, 24 MAY 2022 – AFTERNOON

ELECTRONICS – AS component 1
Principles of Electronics

2 hours 30 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**11**	
2.	**13**	
3.	**15**	
4.	**10**	
5.	**8**	
6.	**7**	
7.	**6**	
8.	**8**	
9.	**13**	
10.	**17**	
11.	**12**	
Total	**120**	

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01

ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen. Do not use gel pen or correction fluid.

You may use a pencil for graphs and diagrams only.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet. If you run out of space, use the additional page(s) at the back of the booklet, taking care to number the question(s) correctly.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in questions **3**(b) and **7**.

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Answer **all** questions.

1. A logic system has two outputs X and Y.

(a) The system gives the following truth table for output X.

C	B	A	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(i) Use the truth table to write down the **unsimplified** Boolean equation for output X in terms of C, B and A. [1]

X = ...

(ii) Complete the Karnaugh map and determine the simplest equation for output X. [3]

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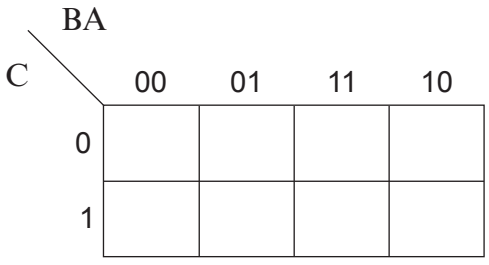

X = ...

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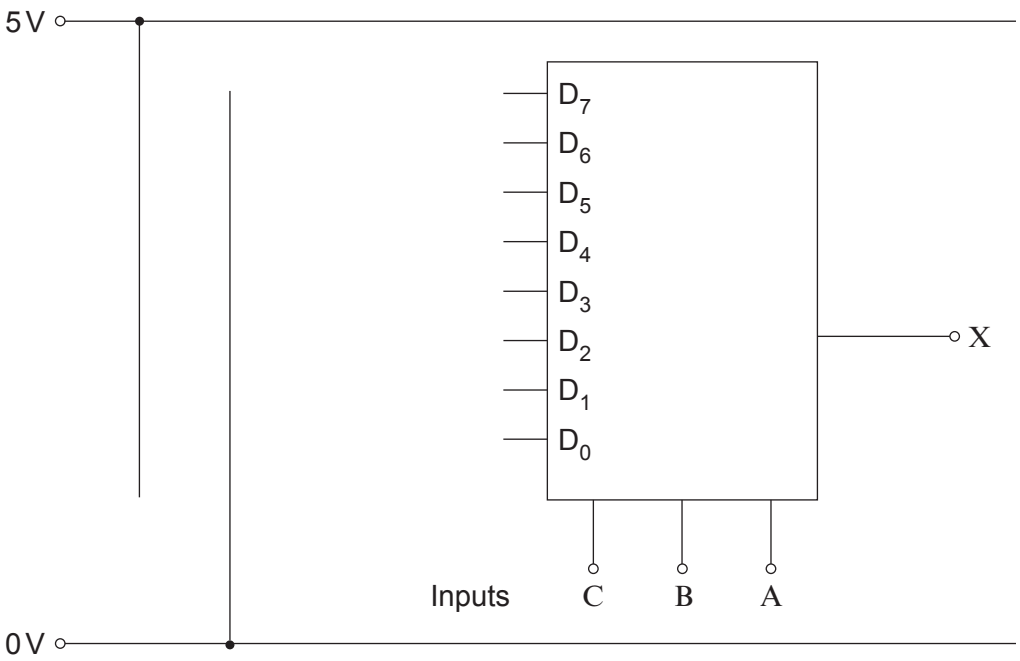
(iii) Draw the logic diagram for X using a combination of NOT, AND or OR gates. [3]

(b) Show how output X could be generated using a multiplexer. [1]



(c) The Boolean equation for output Y is: $Y = \overline{A} + B$

The output Y can be obtained using NAND gates. Draw the logic diagram for output Y and cross out all redundant gates. [3]

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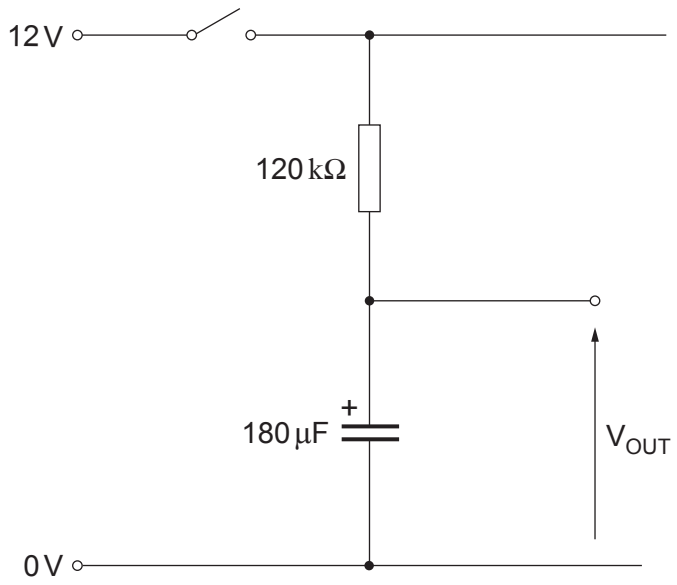
2. The capacitor shown in the following circuit diagram is initially discharged.



(a) The switch is closed at time t = 0.

(i) Determine the time taken for V_{OUT} to increase to 6 V. [3]

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(ii) Calculate the value of V_{OUT} at time t = 30 s. [3]

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(iii) Estimate the time taken for V_{OUT} to reach approximately 12 V. [1]

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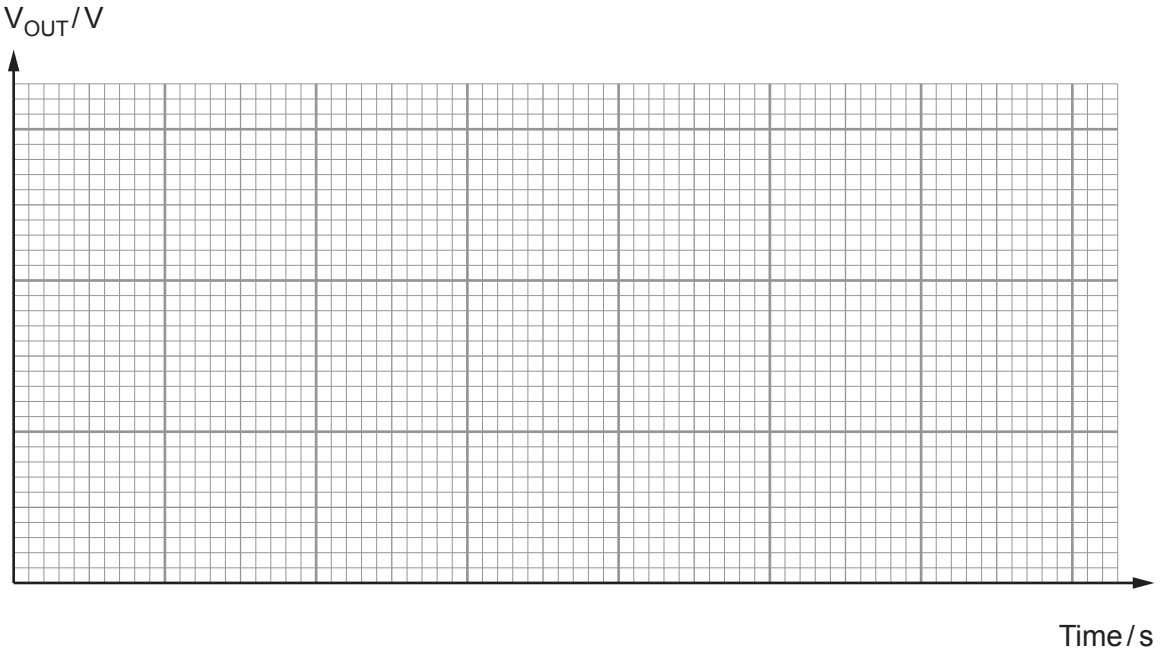
(b) (i) Use your three answers to part (a) to complete the graph of V_{OUT} against time on the axes below. Label both axes with your chosen scales. [3]



(ii) Use the graph to estimate the time taken for V_{OUT} to reach 7.5 V. [1]

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(c) A second, identical capacitor is connected in parallel with the original capacitor.

(i) Calculate the overall capacitance of the altered circuit. [1]

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(ii) Approximately how long will it take for V_{OUT} to reach 7.5 V? [1]

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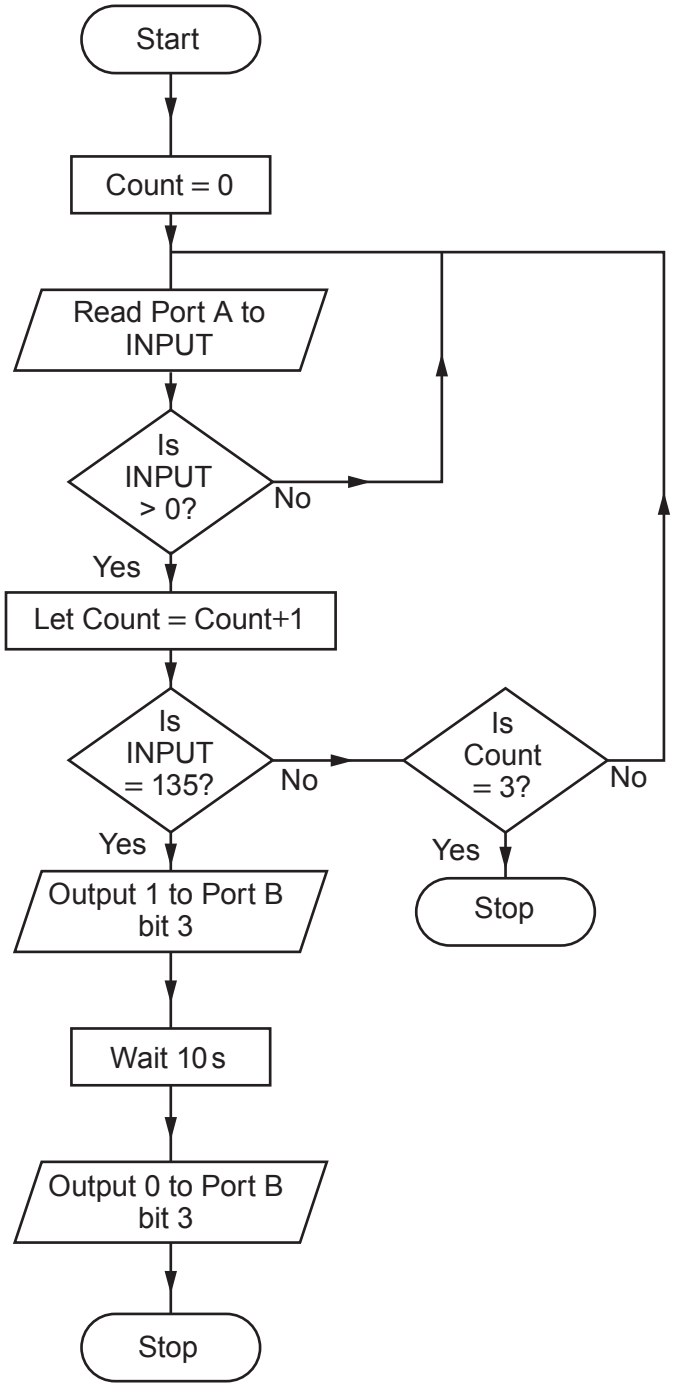
3. (a) Convert the following:

(i) Decimal 135 to Binary (8-bit) ..... [1]

(ii) Binary 01001011 to hexadecimal ..... [1]

The following program forms part of the entry system for a secure room.
An 8-bit binary number corresponding to the decimal 135 is entered via a keypad attached to Port A of a microcontroller.
A solenoid lock is attached to bit 3 of Port B.



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(b) Analyse the flow chart and explain in detail how the program operates. [6 QER]

Turn over.

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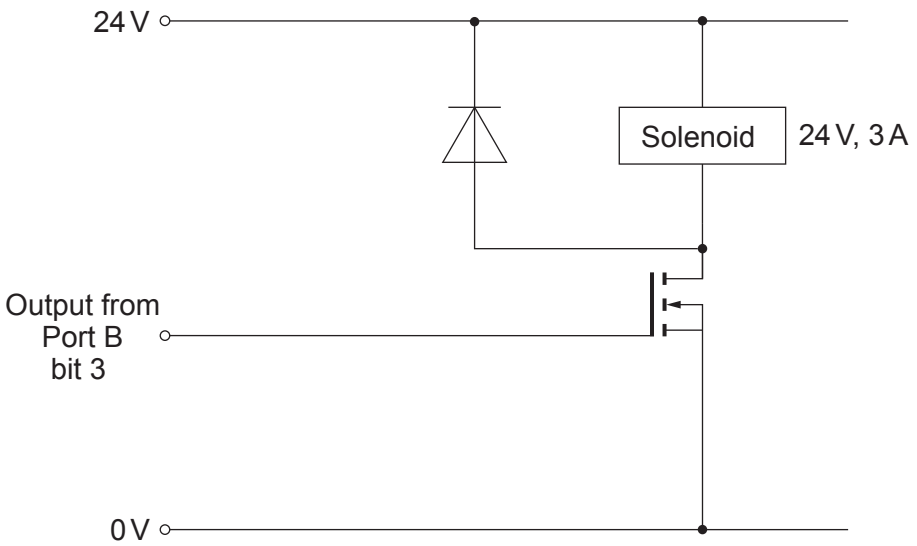
(c) The circuit diagram for the solenoid lock is shown below.



(i) Explain why the diode is needed in this circuit. [1]

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(ii) The MOSFET requires a minimum value of V_{GS} = 5 V for the solenoid to operate at its rated current. Calculate the value of the transconductance g_M. [3]

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(iii) The MOSFET dissipates a power of 1.5 W when the solenoid is operating at its rated current.
Calculate the value of r_{DSon}. [3]

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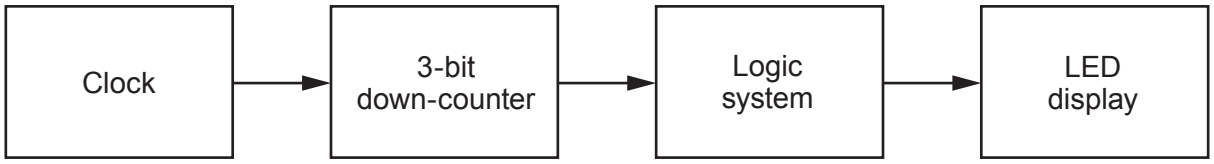
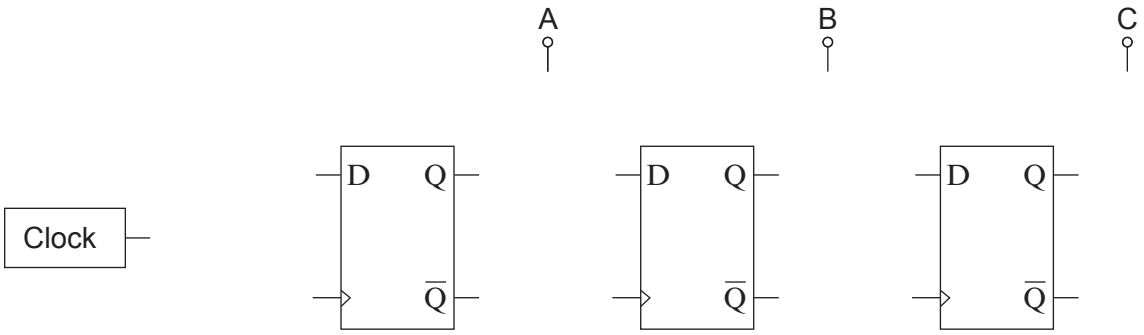
4. A binary down-counter and logic system are used to drive an LED display.



(a) The diagram shows three D-type flip-flops, which form part of a binary down-counter. Outputs A, B and C are used to indicate the binary output. A is the least significant bit.

Complete the diagram to make the 3-bit binary down-counter. [3]



(b) The initial state of the counter is shown in the table. Complete the table, using 0 or 1, to indicate the logic state of each output just after the stated number of clock pulses. [2]

	OUTPUT C	OUTPUT B	OUTPUT A	LED ON
Initial state	1	1	1	RED
After the **3rd** clock pulse				YELLOW
After the **5th** clock pulse				GREEN

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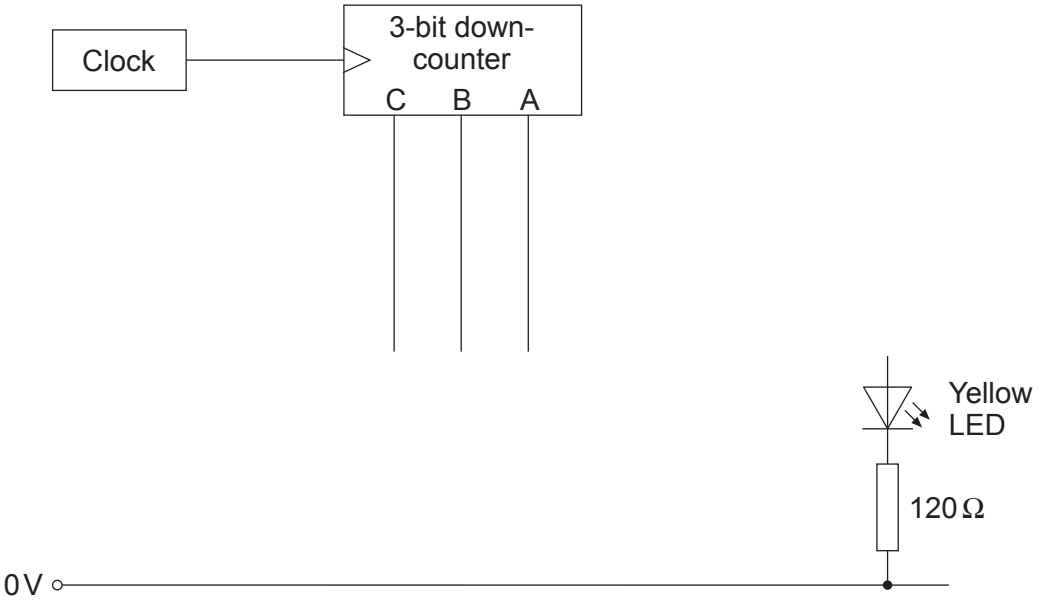
(c) (i) The system is used to light LEDs in sequence. On the diagram below, add the necessary logic gates and connections so that the yellow LED lights on the **3rd pulse only**. [2]



(ii) The forward voltage drop across the LED is 2.1 V. When the output of a logic gate is 5 V, calculate the current that flows through the LED. [3]

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Turn over.

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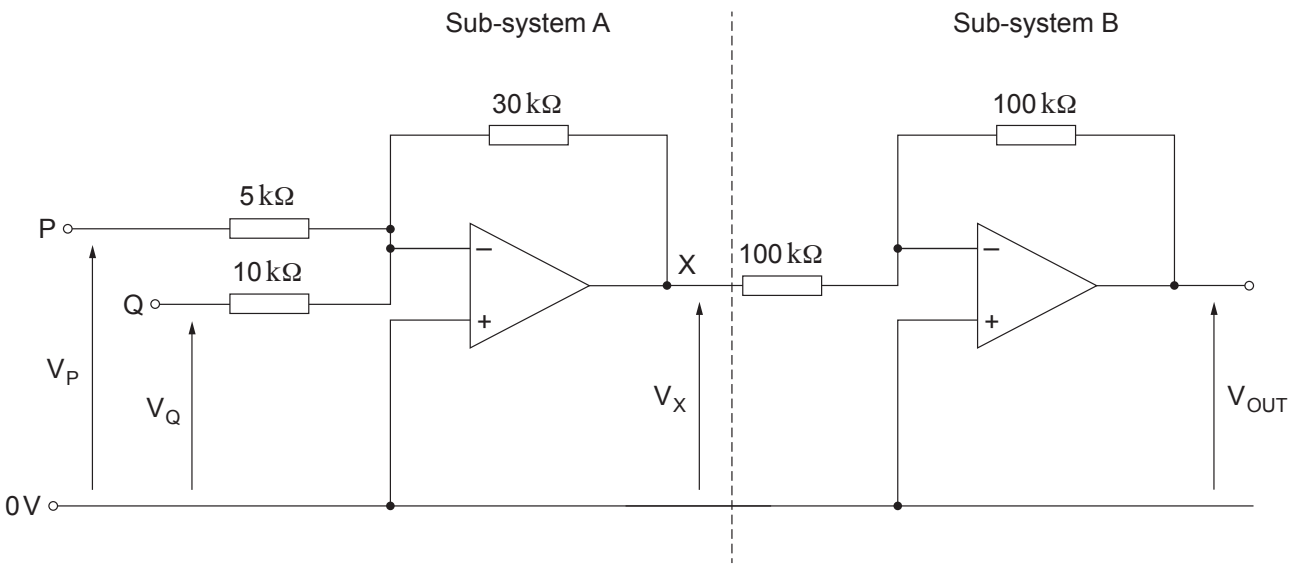
5. The circuit diagram shows a summing amplifier consisting of sub-system A and sub-system B. Both op-amps saturate at ±16 V.



(a) Calculate V_X when $V_P = 1.2$ V and $V_Q = 2.0$ V. [3]

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(b) State the purpose of sub-system B. [1]

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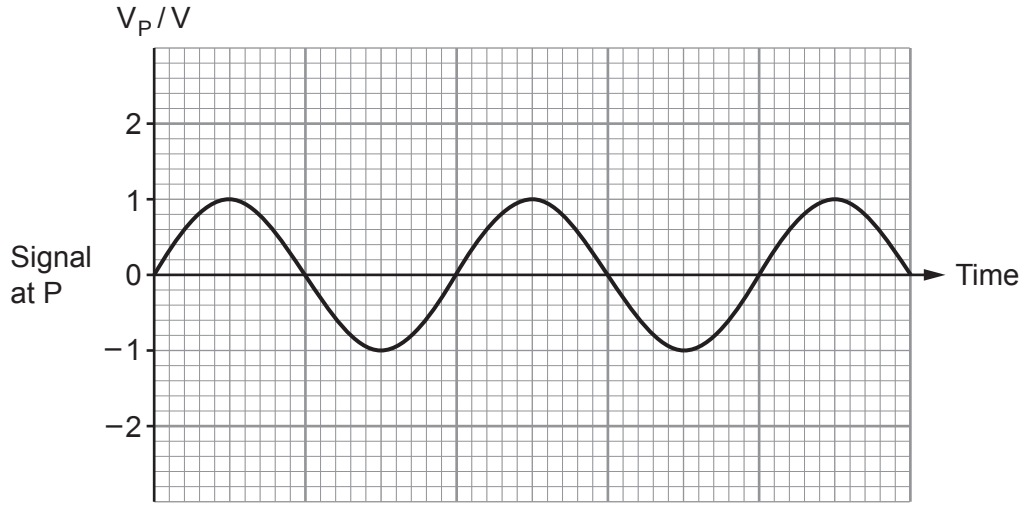
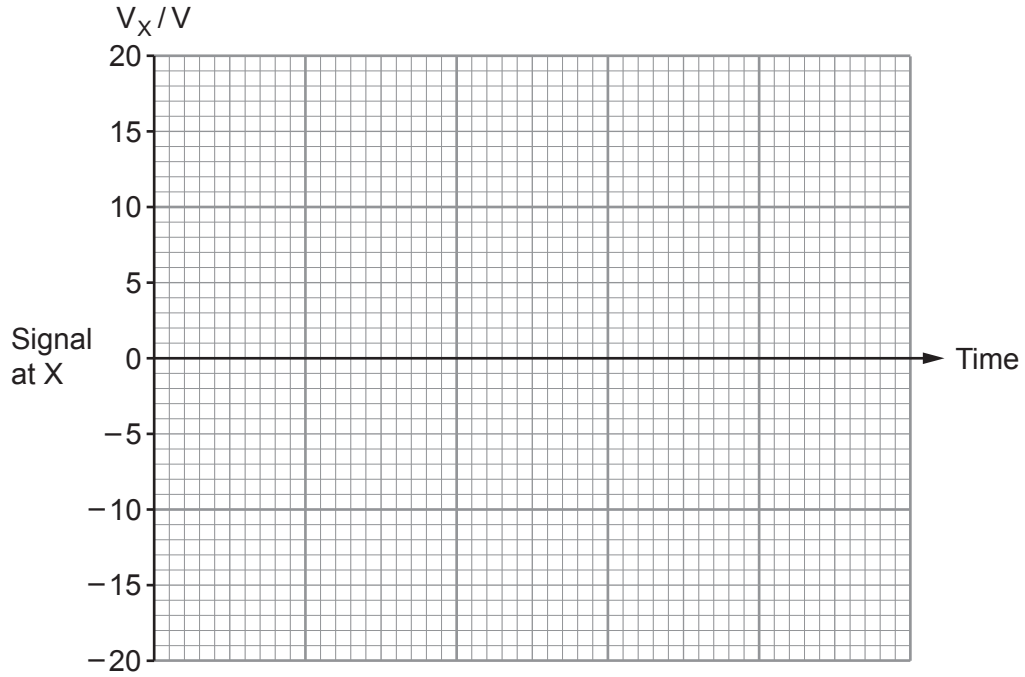
(c) The following signal is applied to input P.





(i) V_Q is set to 0 V. Calculate the amplitude of the signal V_X. [1]

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(ii) V_Q is now set to 2.0 V DC and signal P remains as shown in the top graph. **Draw the graph** of V_X. [3]

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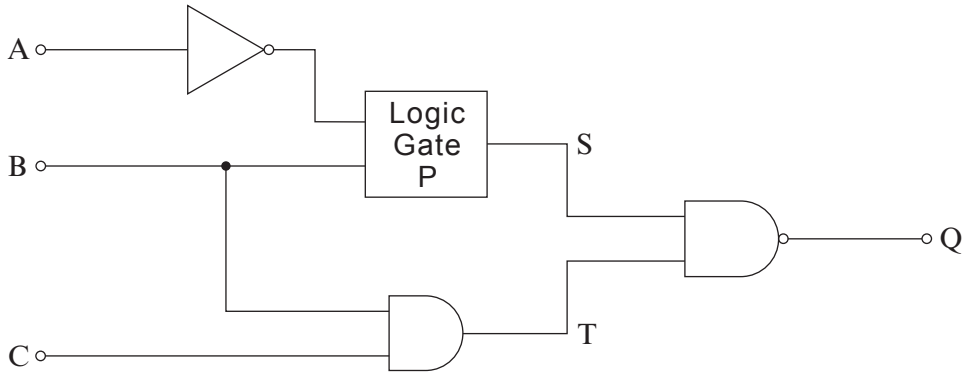
6. The following diagram shows a logic system.



(a) (i) The signal at point S is given by the Boolean equation $S = \overline{(\overline{B} + \overline{A})}$. Identify logic gate P. [1]

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(ii) Write down the Boolean equations for T and Q in terms of inputs A, B and C. [2]

T = ...

Q = ...

(b) An engineer produces the following Boolean equation as a solution to part of a design problem.

$$Q = \overline{(\overline{C + A}) + (\overline{\overline{B}.A})}$$

A colleague suggests that one of the inputs is not needed.
Apply de Morgan's theorem to this equation and simplify it to identify the input that is not needed. [4]

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The input not needed is .....

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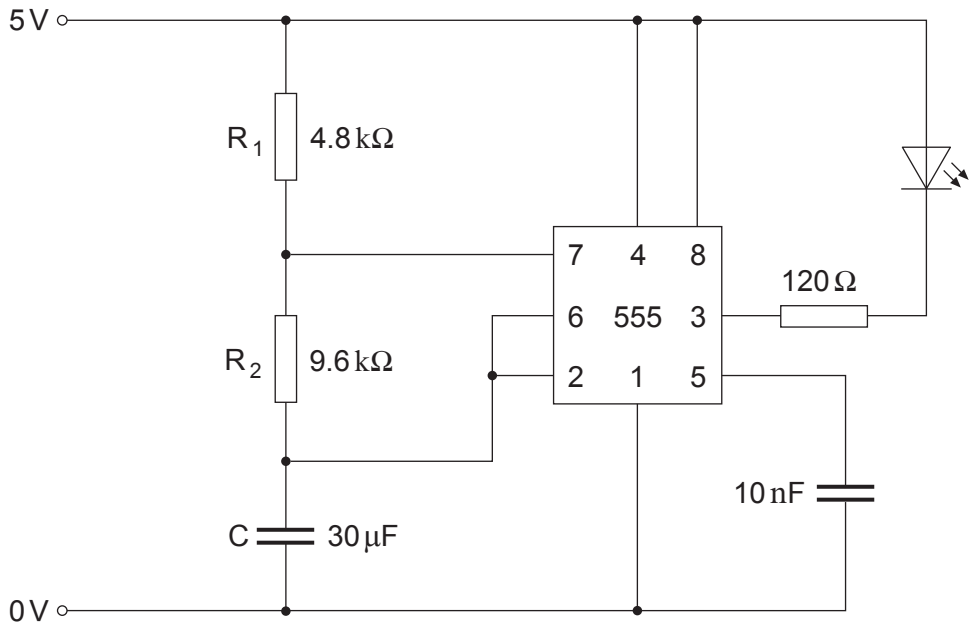
7. An astable system has the following specification.

- A mark:space ratio of 3:2
- A frequency of 0.2 Hz
- The LED is ON for 3 s each cycle.

A design for the system is shown below.



Evaluate the design shown in the diagram against the system specification **and** suggest any improvements required to meet the specification fully. [6 QER]

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8. Transition gates make use of the propagation delay in logic gates.

(a) What is meant by propagation delay? [1]

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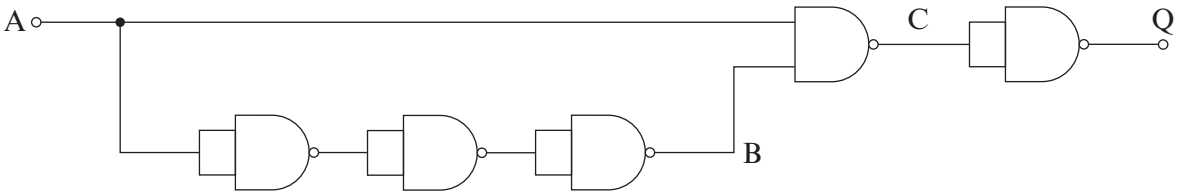
(b) The circuit diagram for a transition gate is shown below. Each logic gate has a 10 ns propagation delay. Assume that the input at A has been at logic 0 for a long time.



The signal shown on the graph opposite is applied to input A.
Show on the graph how the logic levels at B, C and Q change over the course of 80 ns. [5]

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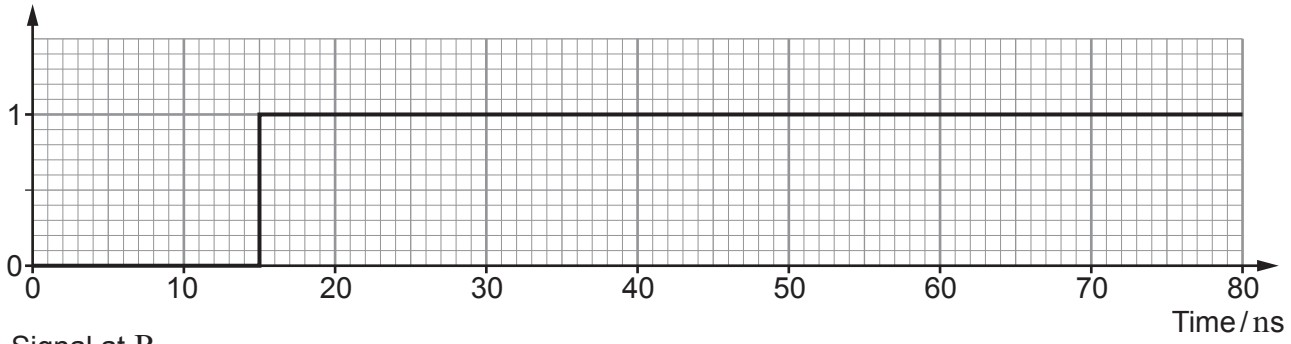
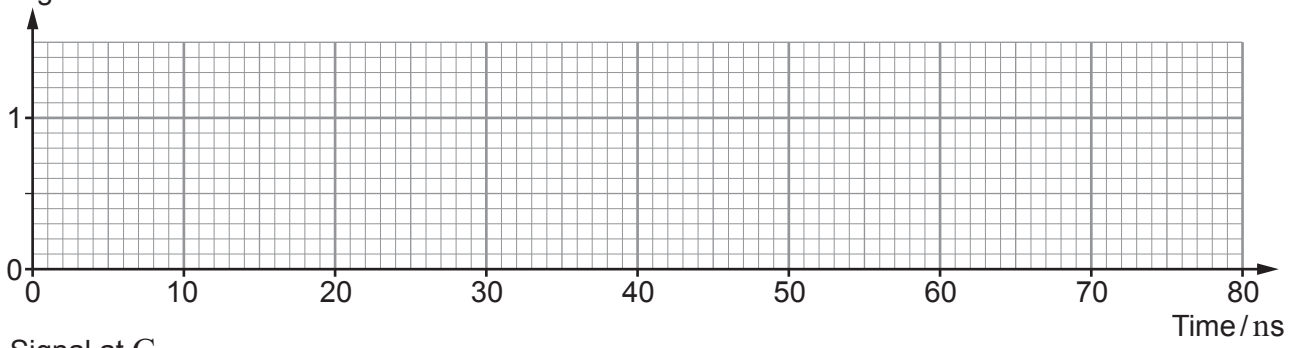
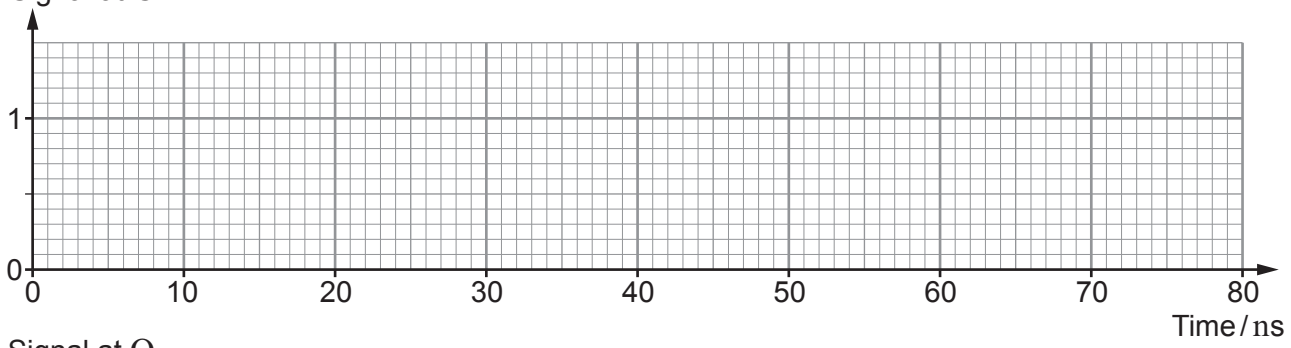
Signal at A



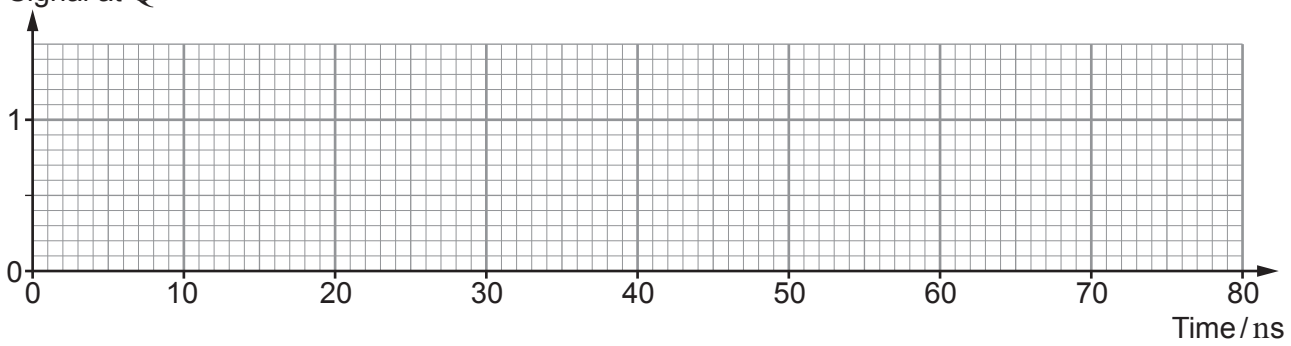
Signal at B



Signal at C



Signal at Q



(c) Describe how the signal at Q would change if NAND gate redundancy was applied to the circuit. [2]

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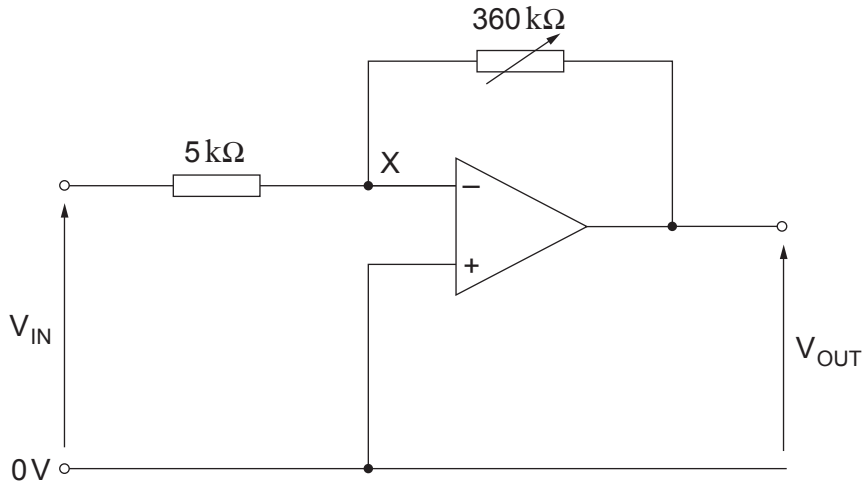
9. An op-amp voltage amplifier uses negative feedback.
In the circuit below the gain can be varied.
The op-amp supply voltage is ±18 V and the output saturates at ±17 V.



(a) State **two** benefits of negative feedback to this circuit. [2]

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(b) When the output of the amplifier is not saturated, point X is a 'virtual earth'. Explain why point X is a 'virtual earth'. [2]

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(c) (i) Calculate the range of the voltage gain. [2]

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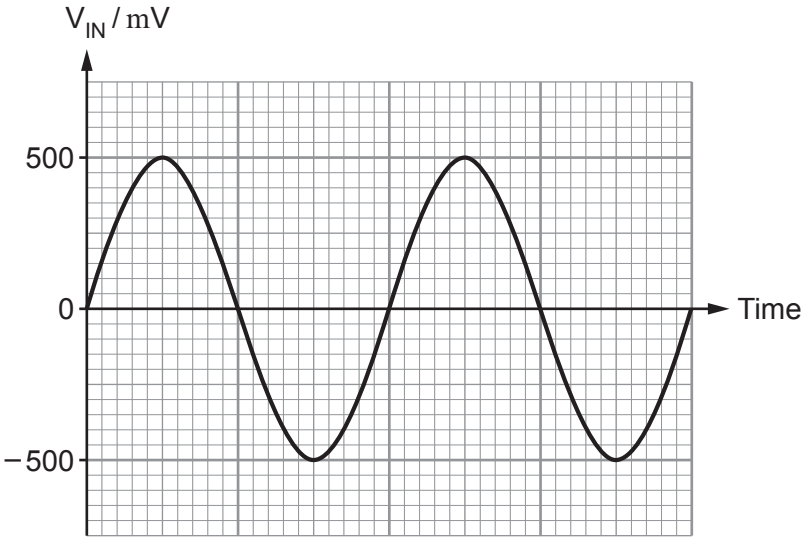
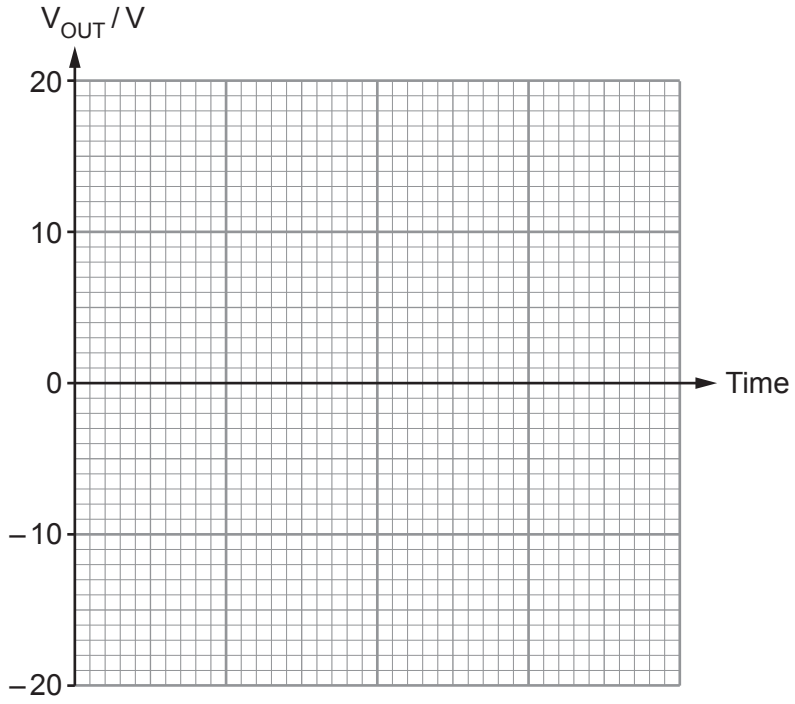
(ii) The feedback resistor is set to give a gain of **–** 40. The following signal is applied to the amplifier input. Draw the output voltage on the axes provided. [3]





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(d) (i) Draw a circuit diagram for an op-amp voltage follower. [2]

(ii) What is the input impedance of this circuit? [1]

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(iii) What is the output voltage from this circuit when a 3.2 V DC input signal is applied? [1]

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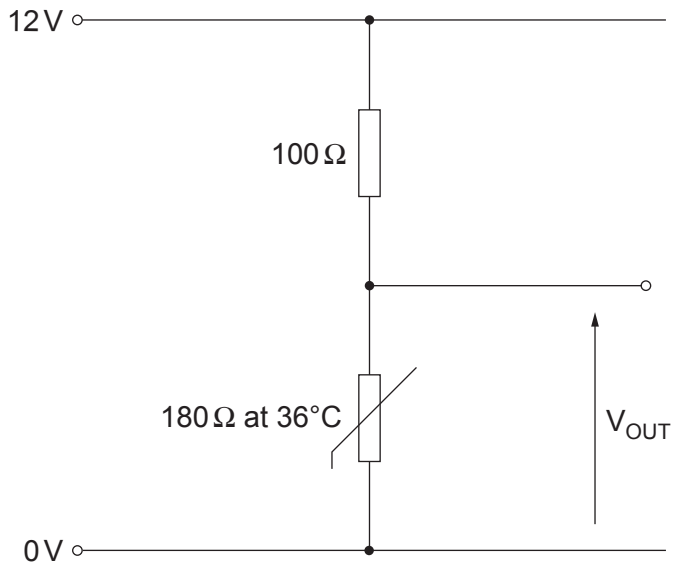
10. A project brief requires a student to design a temperature sensing system that will sound an alarm if a patient's temperature falls below 36 °C. The temperature sensing sub-system is shown below. The resistance of the thermistor is 180 Ω at 36 °C.



(a) (i) Thevenin's theorem is used to produce an equivalent circuit. Calculate the open circuit voltage V_{OC} and the equivalent resistance R_{EQ}. [5]

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(ii) Draw the equivalent circuit. [1]

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(b) An alarm, rated at 6 V, 50 mA, is connected across V_{OUT}. Use the equivalent circuit to show whether the alarm will work as specified. [3]

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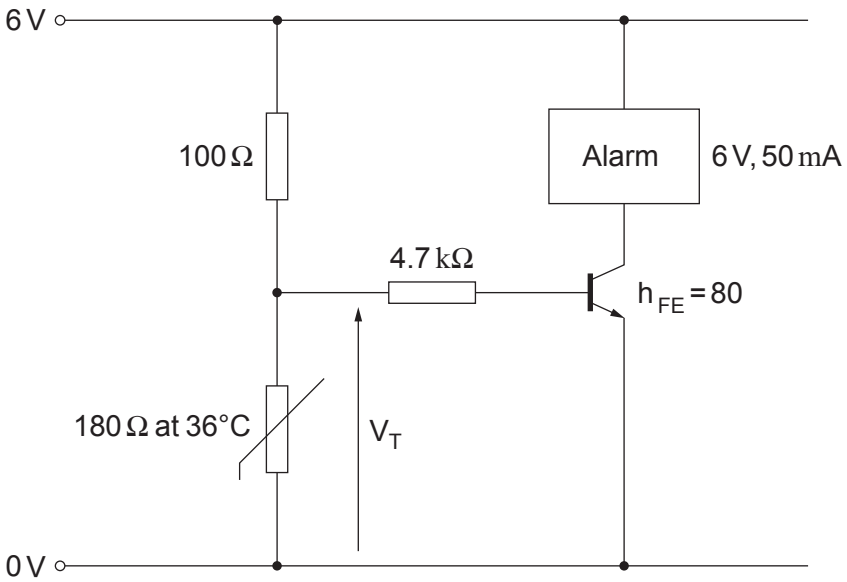
(c) A redesigned circuit diagram is shown below. The power supply is altered to 6 V.



(i) Calculate the value of V_T that will just saturate the transistor. [3]

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(ii) Evaluate whether the alarm will now work as specified. [5]

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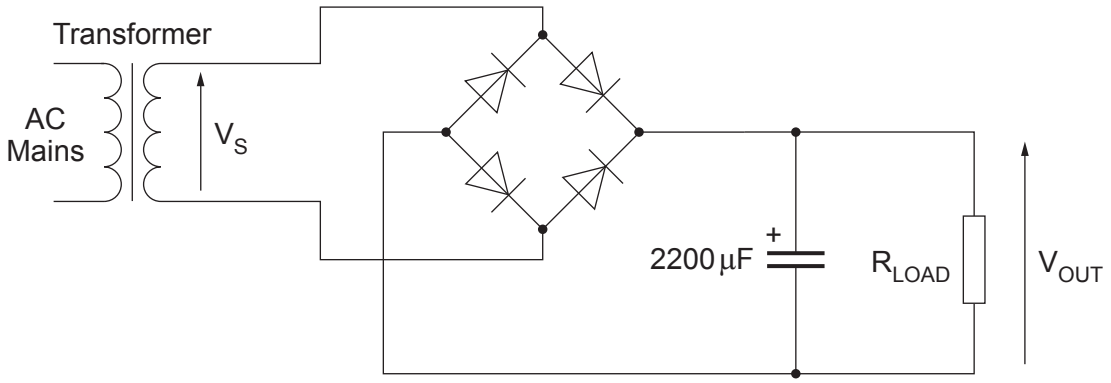
11. The following diagram shows the circuit of a full-wave power supply connected to the 240 V, 50 Hz AC mains.



(a) In the graph below the voltage across the secondary windings of the transformer (V_S) is shown as a dotted waveform and has a peak value of 12 V.

(i) What is the peak value of the voltage V_{OUT}? [1]

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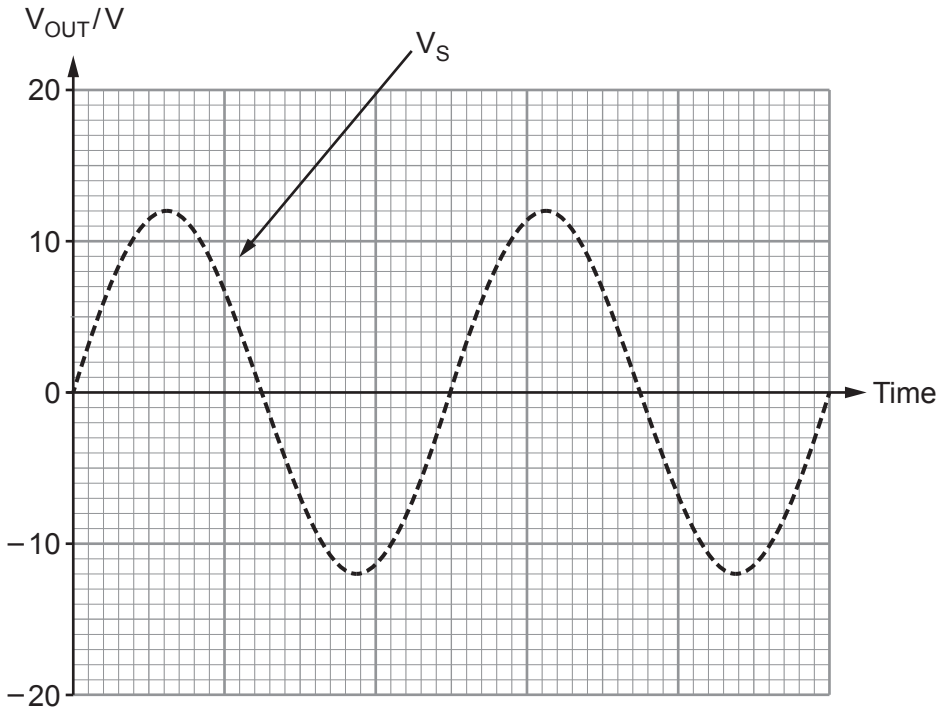
(ii) On the axes provided below sketch the graph to show the output voltage V_{OUT} when a small current flows through load resistor, R_{LOAD}. [3]



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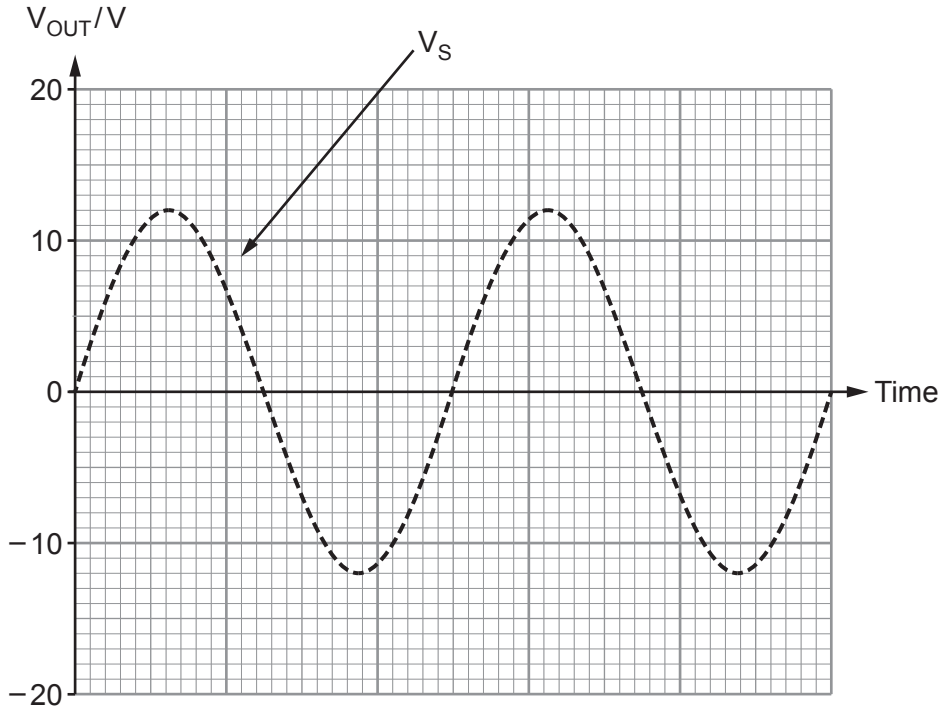
(b) R_{LOAD} is changed to allow a large load current to flow. Use the axes below to sketch the resulting voltage V_{OUT}. [1]



(c) Calculate the maximum load current if the ripple voltage must not exceed 2.8 V. [4]

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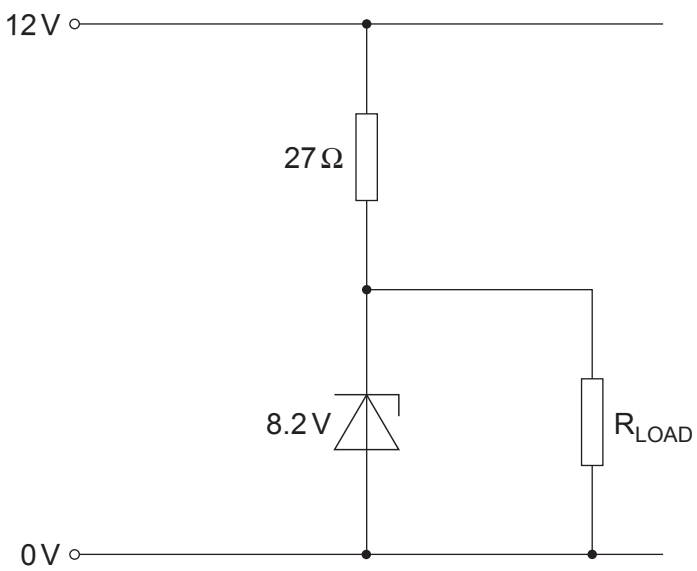
(d) A regulated power supply is shown below. The zener diode requires a minimum current of 10 mA in order to maintain the zener voltage.



Calculate the maximum current through the load, R_{LOAD} whilst maintaining the zener voltage. [3]

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Question number	Additional page, if required. Write the question number(s) in the left-hand margin.

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