Surname	Centre Number	Candidate Number
First name(s)		2

GCE A LEVEL

A490U20-1

Z22-A490U20-1

FRIDAY, 10 JUNE 2022 – MORNING

ELECTRONICS – A level component 2

Application of Electronics

2 hours 45 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**15**	
2.	**20**	
3.	**18**	
4.	**13**	
5.	**6**	
6.	**16**	
7.	**20**	
8.	**16**	
9.	**16**	
Total	**140**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen. Do not use gel pen or correction fluid.

You may use a pencil for graphs and diagrams only.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

If you run out of space, use the additional page(s) at the back of the booklet, taking care to number the question(s) correctly.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

The assessment of the quality of extended response (QER) will take place in question **5**.

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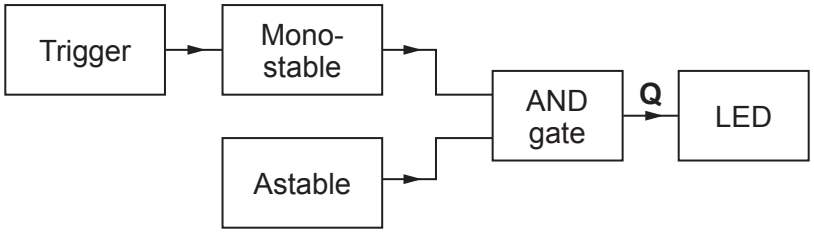
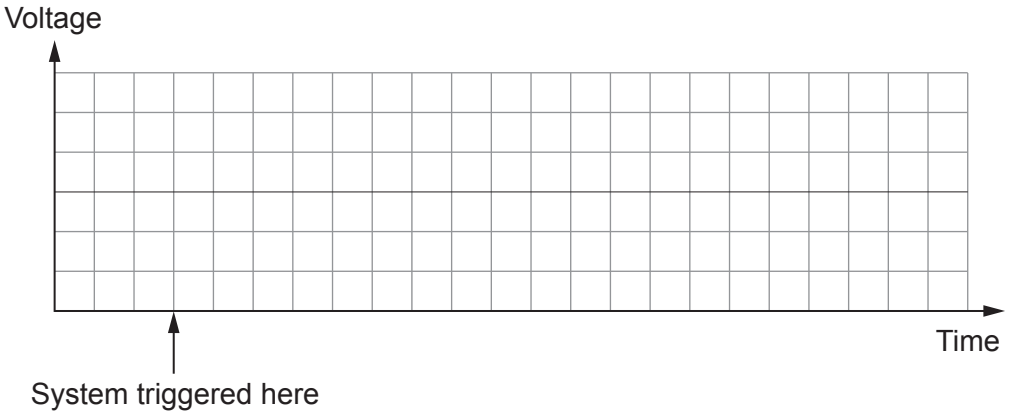
Answer **all** questions.

1. The following system makes an LED flash a number of times when triggered by pressing a switch.



(a) The period of the monostable is three times longer than that of the astable. The astable has a mark:space ratio of 3:2.

The system is triggered at the time shown. Use the axes provided to sketch the signal at **Q**. The sketch should show the signal until the monostable resets. [2]



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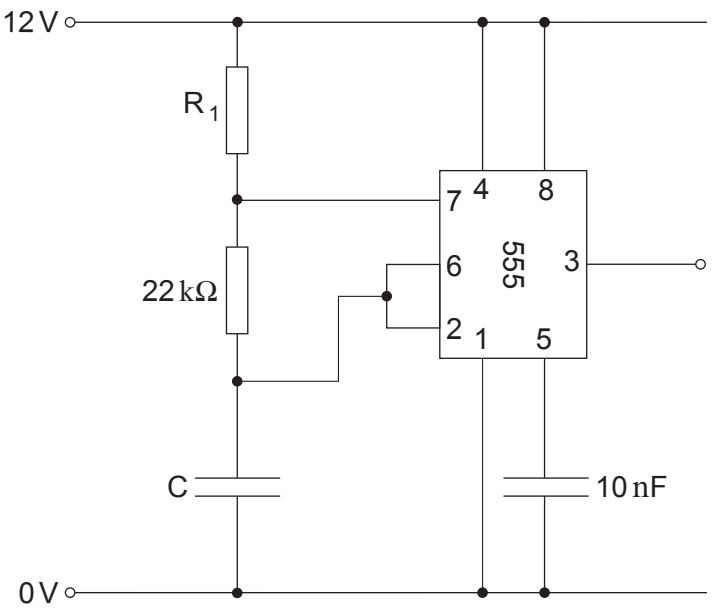
(b) The circuit diagram for the astable is shown below.



(i) The astable has a mark:space ratio of 3:2.
Calculate a suitable value for R_1. [3]

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(ii) **Modify the circuit diagram** by adding an LED and a resistor R_2, connected so that the LED lights when the output of the 555 timer goes high. [2]

(iii) The output of the 555 timer switches between 12 V and 0 V.
The LED has a forward voltage drop of 3.2 V and a forward current of 30 mA when lit. Calculate the ideal value for R_2. [3]

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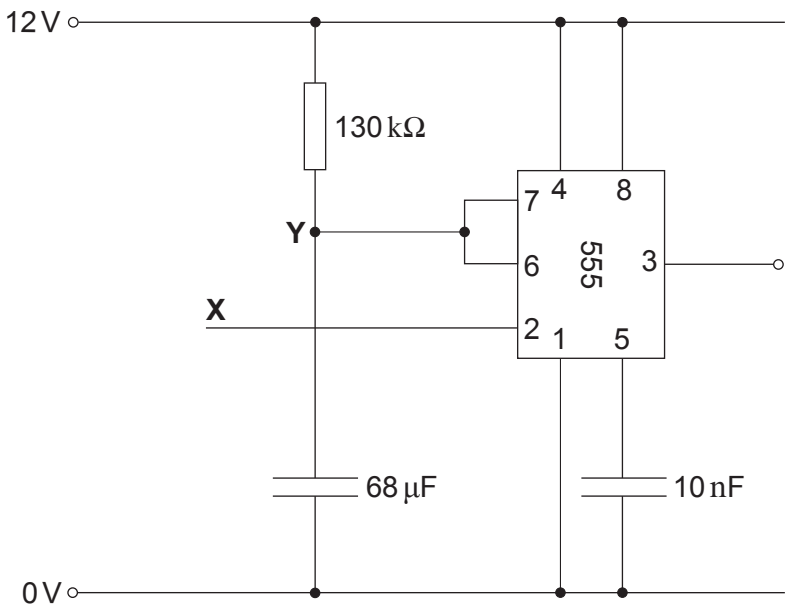
(c) Part of the circuit diagram for the monostable sub-system is shown below.



(i) The monostable is triggered by a falling-edge signal applied at point **X**. **Complete the circuit diagram** by adding a switch and any other components needed to trigger the monostable. [2]

(ii) Calculate the time period of the monostable. [3]

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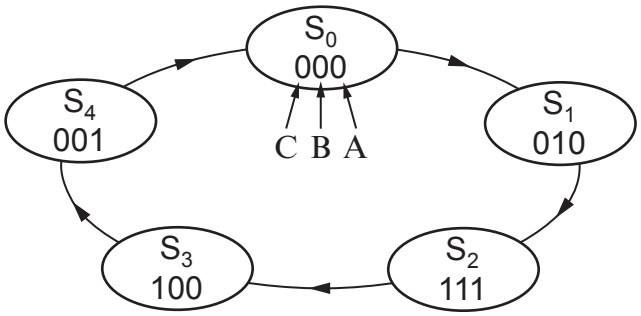
2. In a bakery, ingredients are added to a mixing vessel through two valves, B and C.

Periodically, they are mixed by a paddle driven by an electric motor, A, and the vessel is emptied by opening valve X. This sequence then repeats.

The valves are opened and the motor switched on when a logic 1 signal is received.

The control sequence for devices C, B and A is described in the following state diagram:



This control sequence is generated by a system of D-type flip-flops.

(a) Use the state diagram to complete the following table. In addition to the signals within the system of D-type flip-flops, it also shows the signal sent to valve X.
The main sequence contains five states. The table also shows the behaviour of the unused states. [2]

State	Current state			Next state			Valve X
	Valve C	Valve B	Motor A	D_C	D_B	D_A	
S_0	0	0	0				0
S_1							0
S_2							0
S_3							0
S_4							1
S_5	0	1	1	1	0	0	0
S_6	1	0	1	0	0	0	0
S_7	1	1	0	1	0	1	0

(b) The sequence is controlled by clock pulses from a pulse generator having a frequency of 0.2 Hz.
For how long is valve B open in each cycle of the sequence? [2]

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(c) Determine Boolean expressions linking signals D_C, D_B and D_A to the signals that control C, B and A. [7]

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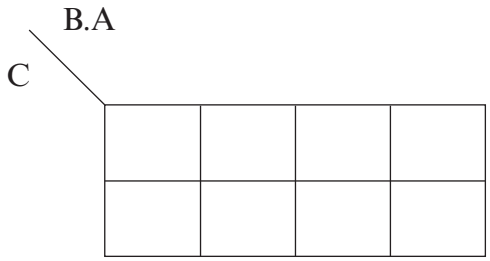
D_C = ...



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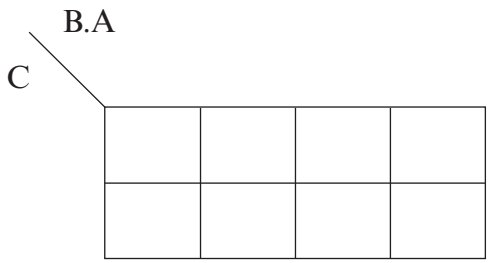
D_B = ...



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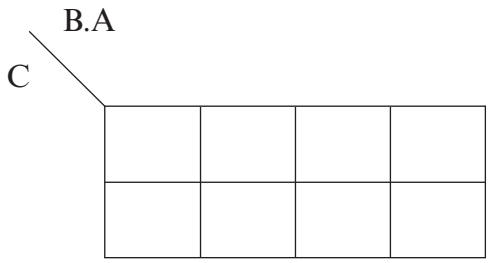
D_A = ...



(d) Determine if there are any stuck states. Explain how you arrive at your answer. [2]

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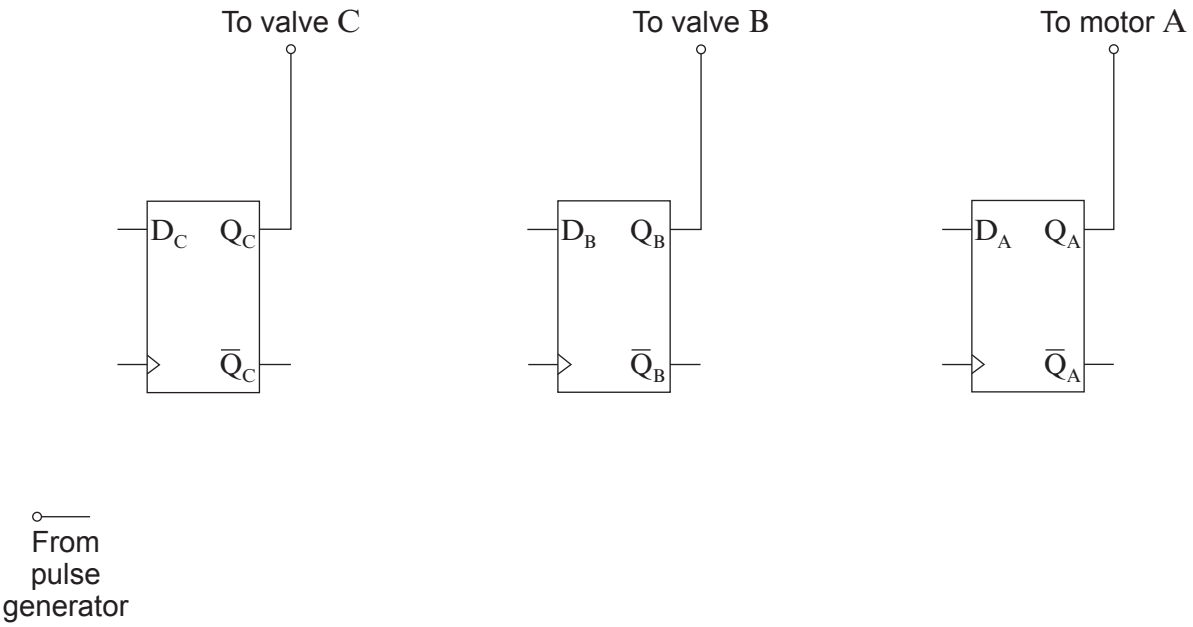
(e) Complete the circuit diagram for the system of D-type flip-flops. [5]



(f) A logic system uses the output signals from the D-types to control valve X.

(i) Determine the Boolean expression for X in terms of outputs C, B and A. [1]

X = ...

(ii) What is the minimum number of additional gate(s) required to generate output X? [1]

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3. The same bakery decides to upgrade the control system. As part of the new system, a microcontroller is used to control valves B, C and X and motor A.

(a) What is the purpose of the registers? [2]

PORTB .....

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TRISB .....

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(b) (i) Valve B is connected to port B, bit 2.
Valve C is connected to port B, bit 3.
Motor A is connected to port B, bit 4.
Valve X is connected to port B, bit 5.
The valves are opened and the motor switched on by a logic 1 signal from the microcontroller.
Complete the following instructions to close valves B and C, switch on motor A and open valve X: [2]

movlw b'.....'

..... PORTB

(ii) The same operation could have been carried out using the instructions clrf and bsf. Show how this could be done: [3]

clrf .....

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(c) The program includes a delay subroutine called 'delay1'.
Part of this is listed below:

```
150                 movlw   d'100'
151                 movwf   count
152     repeat      decfsz  count,1
153                 goto    repeat
154                 return
```

(i) What is the effect of changing line 150 to [1]

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150                 movlw   d'120' ?
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(ii) Explain what is happening in lines 152 to 154. [4]

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(d) A temperature-sensing unit is attached to motor A. If the motor overheats, the sensing unit triggers an external hardware interrupt, using the interrupt pin, pin 6.

(i) Describe the role of the "stack" when an interrupt occurs. [2]

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(ii) Interrupts are controlled by the Interrupt Control Register, (INTCON). Complete the table to show the contents of the INTCON register when external (port B) interrupts are enabled and the external interrupt flag is cleared. [3]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

(e) Describe **one** advantage of controlling the bakery mixer with the microcontroller system instead of with the sequence generator made from D-type flip-flops. [1]

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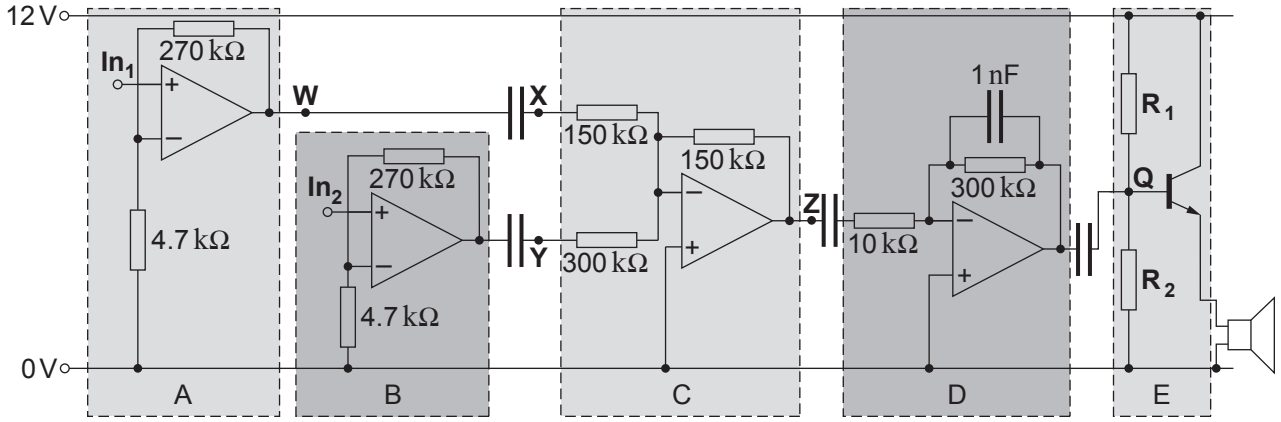
4. The circuit diagram for an audio system is shown in the diagram.
It has two inputs labelled $\mathbf{In_1}$ and $\mathbf{In_2}$.



(a) In this audio system, which block (A, B, C, D or E) is: [2]

(i) a pre-amplifier? .....

(ii) a power amplifier? .....

(b) Assuming that all the op-amps have ideal characteristics, what is the input impedance of the sub-system in: [2]

(i) block A? .....

(ii) block D? .....

(c) Several tests are performed on the system:

(i) A steady DC signal of 10 mV is applied to $\mathbf{In_1}$.

What is the voltage at point **W**? [3]

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(ii) Inputs $\mathbf{In_1}$ and $\mathbf{In_2}$ are now set to 0 V and test signals are applied to points **X** and **Y**. The signal applied at **X** is 20 mV DC and the signal applied to **Y** is 60 mV DC.

Calculate the voltage at point **Z**. [2]

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(d) (i) What is the most appropriate DC voltage at point **Q**? [1]

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(ii) State why this is the most appropriate DC voltage at **Q**. [1]

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(e) Explain the role of the decoupling capacitor between blocks **C** and **D**. [2]

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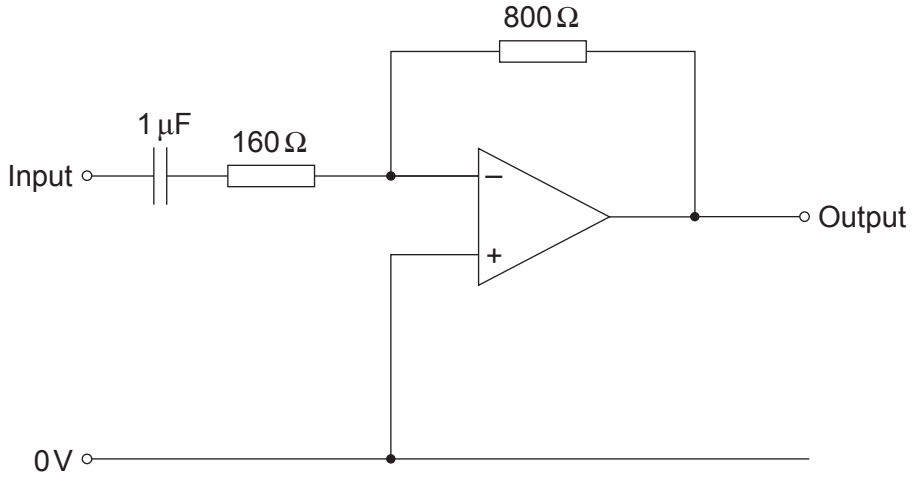
5. A student wishes to use an active filter to boost the bass frequencies of music played on a mobile phone.

The specification for the filter is:

- high frequency gain = 5
- break frequency = 200 Hz

The proposed design is shown in the circuit diagram below:



Evaluate the design to see if it meets the requirements given above and suggest any necessary improvements. [6 QER]

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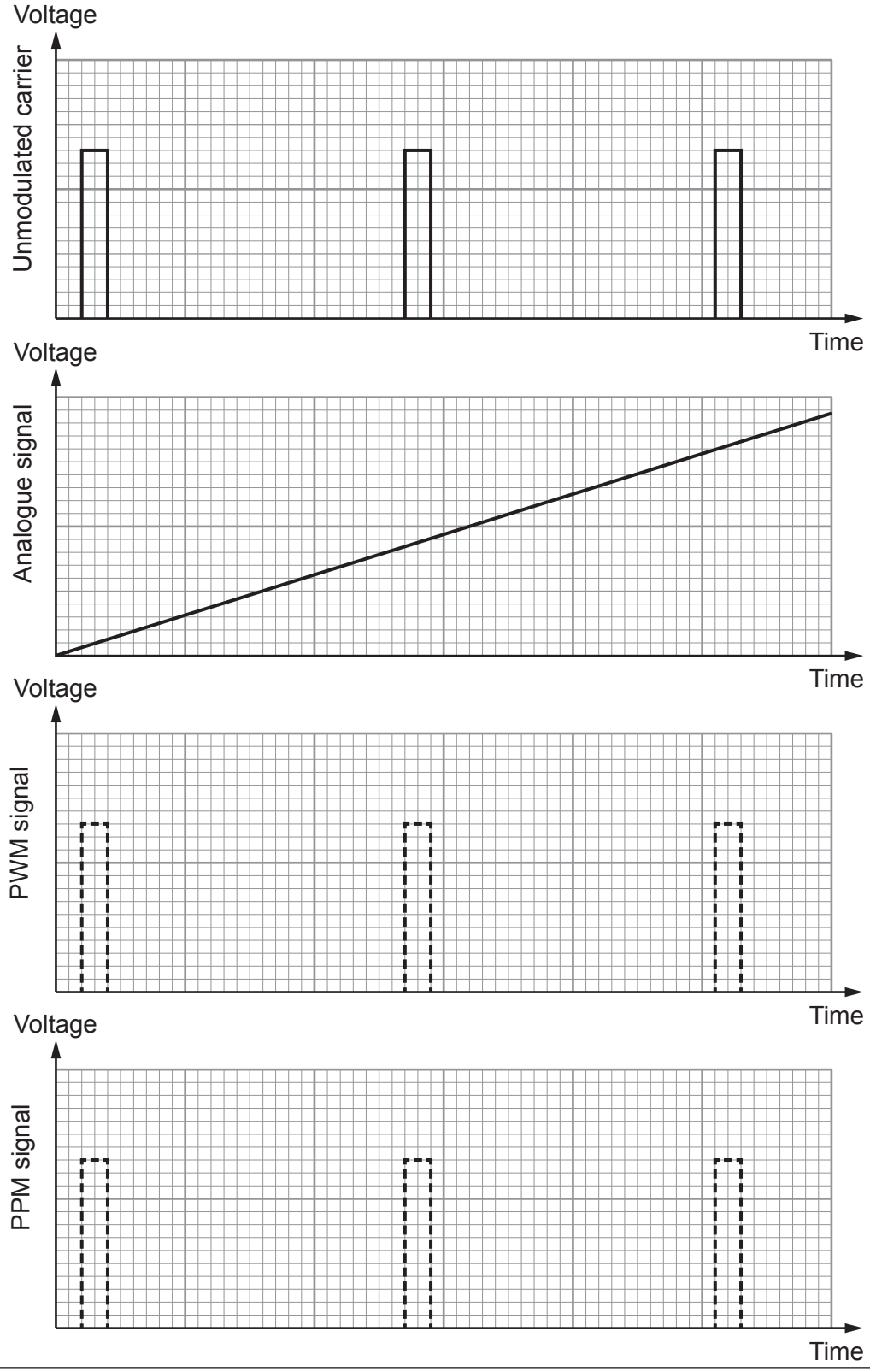
6. (a) An analogue signal can be modulated onto a stream of pulses using pulse width modulation (PWM) or pulse position modulation (PPM).

Use the lower two axes provided to show the effect of modulating the carrier with the analogue signal shown, using these techniques.
The unmodulated carrier is shown using dashed lines to assist you. [4]



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(b) A PCM communication system consists of a transmitter, a communication link and a receiver.

(i) Draw the block diagram for the transmitter, using the following sub-systems:

ADC sampling gate PISO shift register 4 kHz clock low-pass filter 1 MHz clock [2]

(ii) For this PCM system: [3]

I. Which block(s) produce a PAM output signal?

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II. What is the highest signal frequency that can be processed accurately?

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III. Which sub-system cuts out frequencies greater than this?

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(iii) The PCM system is designed for an analogue input signal voltage range of 0 to 10 V. The resolution must be better than 0.01 V.

What is the minimum number of bits required for the ADC? [3]

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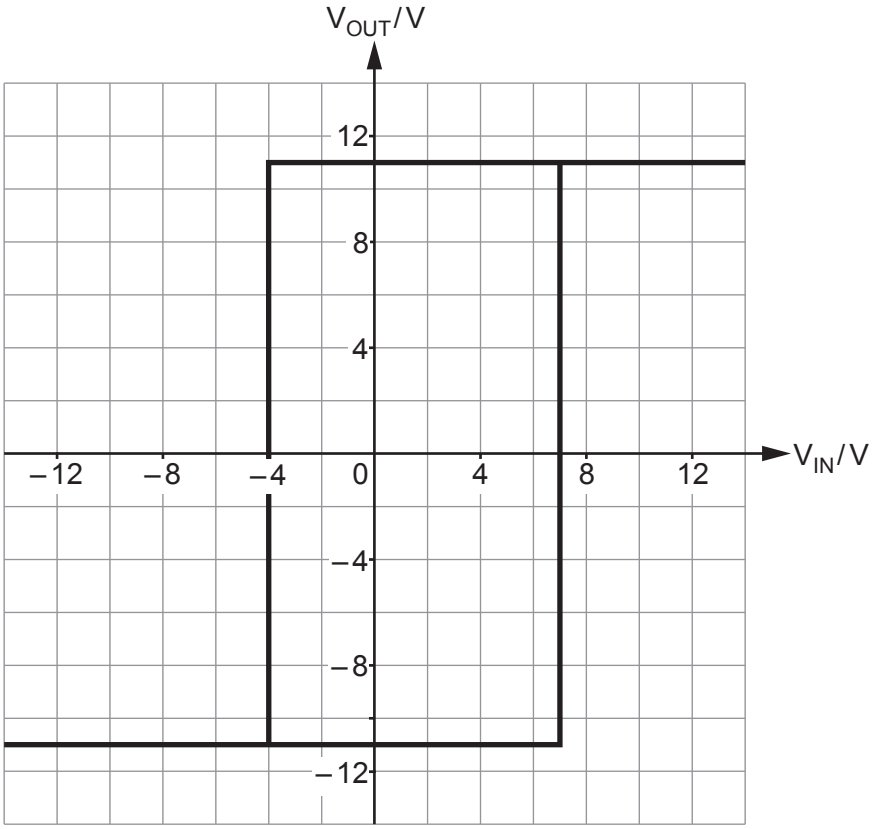
(c) The PCM receiver includes a Schmitt trigger circuit.
The graph shows the voltage transfer characteristic for this sub-system.



(i) Giving details of all the voltages involved, describe what happens to the output voltage of the Schmitt trigger as the input voltage rises from –12V to +12V. [2]

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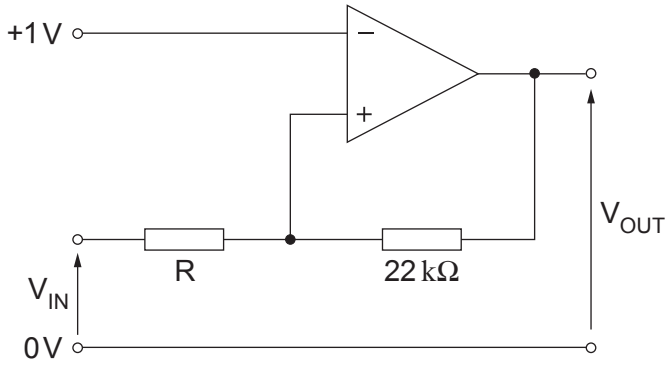
(ii) The circuit diagram for this Schmitt trigger is shown below.



Calculate a suitable value for resistor R. [2]

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7. Optical fibre communication systems use either single-mode or multi-mode optical fibre cables.

(a) (i) Distinguish between single-mode and multi-mode optical fibres in terms of their structure. [1]

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(ii) Describe the relative advantages of single-mode and multi-mode optical fibres in a communication network. [3]

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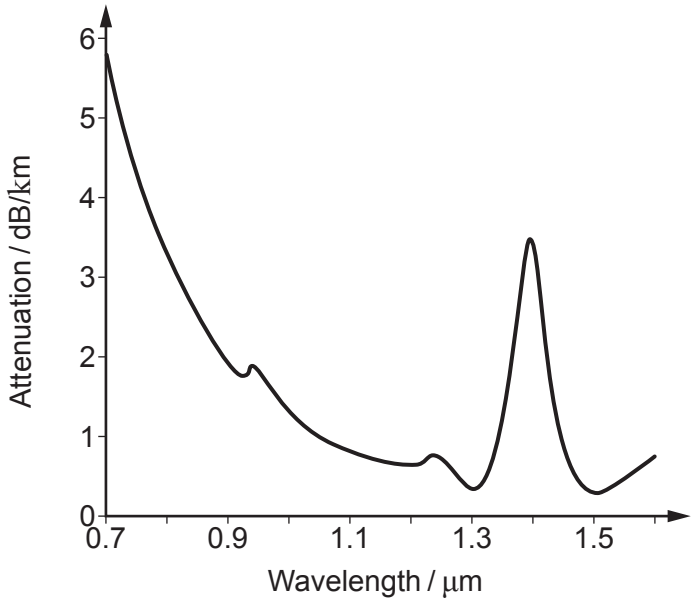
(b) The graph below shows one property of the glass used in an optical fibre.



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(i) This optical fibre communication system uses channels centred on a wavelength of 1550 nm. What is the reason for this? [1]

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(ii) Determine the bandwidth available between wavelengths of 1535 nm and 1565 nm. Assume that electromagnetic waves travel at $2 \times 10^8 \, \text{m s}^{-1}$ in the optical medium. [4]

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(iii) Wave-division multiplexing (WDM – a form of frequency division multiplexing) is used to increase the channel capacity.

Determine the maximum number of channels available between these wavelengths when the channel bandwidth is 18 GHz. [2]

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(c) (i) A 1550 nm laser diode has an average optical power output of 3 W.
It generates 6000 pulses per second, each lasting 500 ns.

Calculate the power delivered by each pulse. [3]

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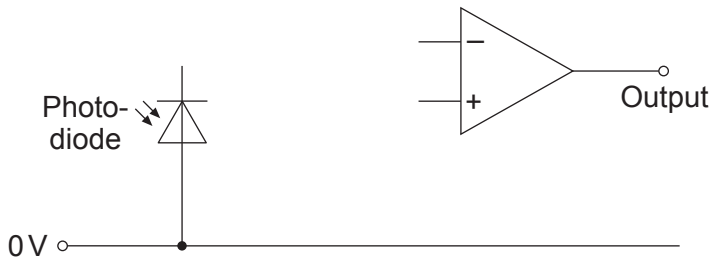
(ii) A current-to-voltage converter is used to generate the output voltage for the optical communications system.

I. Complete the circuit diagram by:
- adding a 30 kΩ resistor;
- connecting the photodiode to the correct input of the op-amp;
- making any other necessary connections. [3]



II. Calculate the output voltage when the photodiode passes a current of 0.2 mA. [3]

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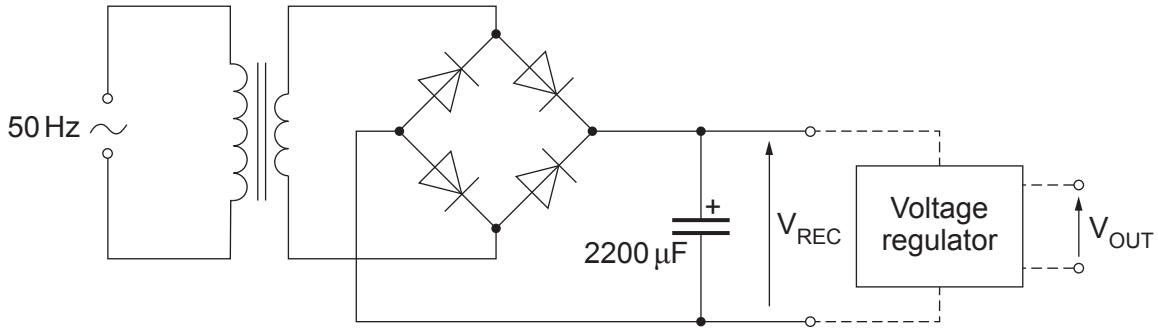
8. (a) Complete the following statements: [2]

(i) ..... regulation is the extent to which the output voltage of a power supply is immune to changes in the output current.

(ii) ..... regulation is the extent to which the output voltage of a power supply is immune to changes in the supply voltage.

(b) Part of the circuit diagram for a regulated power supply is shown below:



Design a voltage regulator to produce an output voltage of 12 V.

Your design must include:
- a 10 V zener diode;
- a 10 kΩ feedback resistor (R_F);
- an op-amp;
- a npn transistor;
- and other necessary components.

(i) Complete the circuit diagram for your design. [4]

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(ii) The full-wave rectifier output V_{REC} = 18 V.
The zener diode requires a minimum current of 10 mA to keep it in reverse breakdown. The voltage regulator is designed so that the current through the zener is 40 mA.

Calculate the ideal values of all fixed resistors used in the circuit and then select suitable practical values from the E24 series.

Label them on the diagram with their E24 values. [8]

(iii) A load is connected to the output of the power supply and draws an appreciable current.

I. What effect would this have on the current through the zener diode? [1]

II. Explain why this happens. [1]

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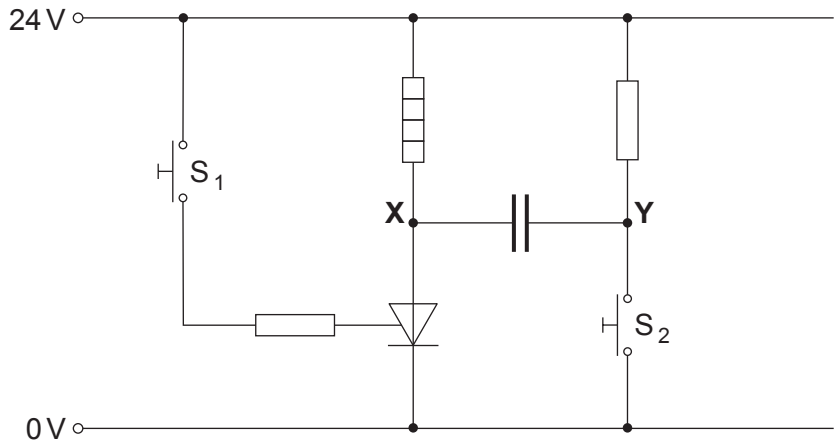
9. (a) A thyristor is used to control the output of a 100 W heater in the following DC switching circuit.



(i) Switch S_1 is pressed momentarily and the thyristor begins to conduct. Give the condition needed to make a thyristor **stay** in conduction. [1]

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(ii) Explain why pressing switch S_2, momentarily, causes the thyristor to cease conduction. Your answer should describe the voltages at **X** and **Y** before and after S_2 is pressed. [4]

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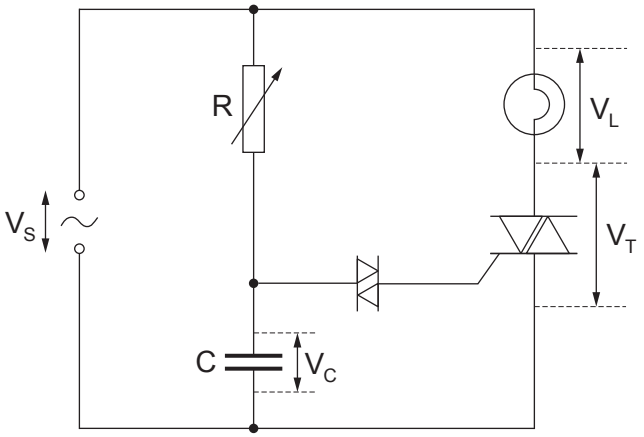
(b) The following circuit is used to control the brightness of a high-power lamp.



(i) State **one** advantage of using a triac over a thyristor in this circuit and explain its significance. [2]

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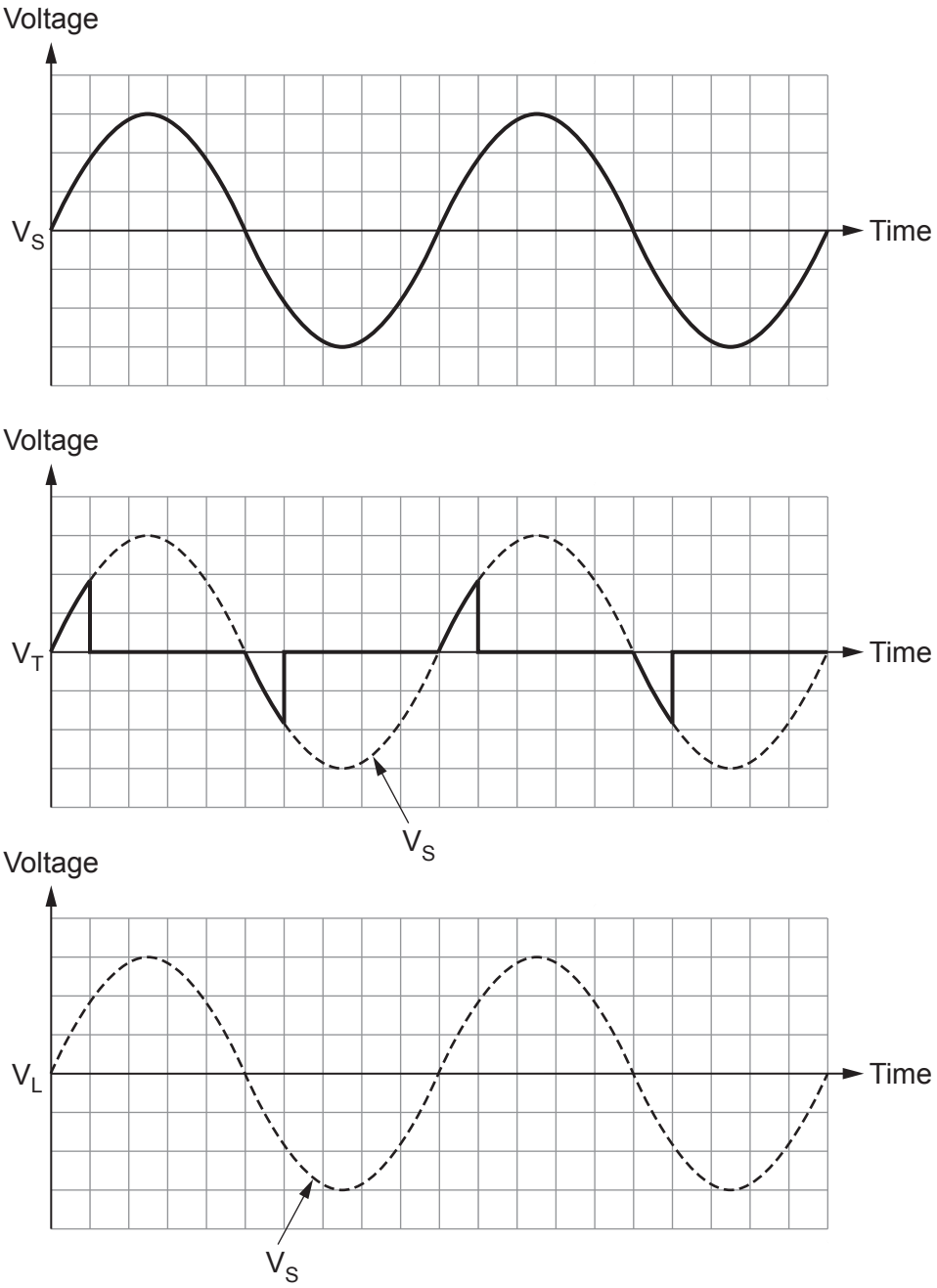
(ii) The upper graph shows the AC supply voltage, V_S. The middle graph shows the voltage, V_T, across the triac.

I. **Label with 'X'**, any time on the middle graph at which the triac is conducting. [1]

II. Use the axes provided to sketch the corresponding voltage, V_L, across the lamp. (The AC supply voltage is shown as a dashed trace.) [2]



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(c) (i) The capacitor, C, has a capacitance of $0.33\,\mu F$ and the variable resistor, R, is set to a resistance of $22\,k\Omega$.
Calculate the phase angle between the voltage across the capacitor, V_C, and the supply voltage, V_S, when the frequency of the AC supply is 50 Hz. [4]

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(ii) The resistance of R is reduced. As a result, the brightness of the lamp increases.
Explain why this happens. [2]

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