Surname	Centre Number	Candidate Number
Other Names		0

GCSE

4162/01

ELECTRONICS

UNIT E2
(Paper version of on-screen assessment)

A.M. WEDNESDAY, 5 June 2013

1 hour

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**2**	
2.	**2**	
3.	**3**	
4.	**2**	
5.	**3**	
6.	**1**	
7.	**2**	
8.	**2**	
9.	**2**	
10.	**4**	
11.	**2**	
12.	**2**	
13.	**1**	
14.	**3**	
15.	**4**	
16.	**5**	
17.	**2**	
18.	**1**	
19.	**3**	
20.	**3**	
21.	**4**	
22.	**3**	
23.	**1**	
24.	**1**	
25.	**2**	
Total	**60**	

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ADDITIONAL MATERIALS

In addition to this paper you may need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

INFORMATION SHEET FOR UNIT E2

This information may be of use in answering the questions.

1. Resistor Colour Codes

BLACK	**0**	**GREEN**	**5**
BROWN	**1**	**BLUE**	**6**
RED	**2**	**VIOLET**	**7**
ORANGE	**3**	**GREY**	**8**
YELLOW	**4**	**WHITE**	**9**

The fourth band colour gives the tolerance as follows:

GOLD ± 5%

SILVER ± 10%

2. Preferred Values for Resistors – E24 series

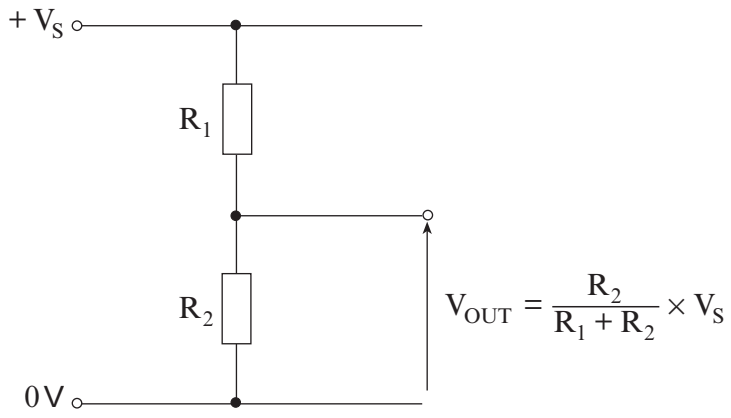
10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

3. Resistance = $\frac{\text{voltage}}{\text{current}}$; $R = \frac{V}{I}$.

4. Effective resistance, R, of two resistors R_1 and R_2 in series is given by $R = R_1 + R_2$.

5. Effective resistance, R, of two resistors R_1 and R_2 in parallel is given by $R = \frac{R_1 R_2}{R_1 + R_2}$.

6. Voltage Divider



7. Power = voltage × current; $P = VI = I^2R = \frac{V^2}{R}$.

8. LED The forward voltage drop across an LED is 2 V.

9. NPN Transistors (i) Current gain = $\frac{\text{Collector current}}{\text{Base current}}$; $h_{FE} = \frac{I_C}{I_B}$.

(ii) The forward voltage drop across the base emitter junction is 0·7 V.

10. Amplifiers

Voltage gain: $A = \frac{V_{OUT}}{V_{IN}}$

Non-inverting amplifier: $A = 1 + \frac{R_F}{R_1}$

Inverting amplifier: $A = -\frac{R_F}{R_{IN}}$

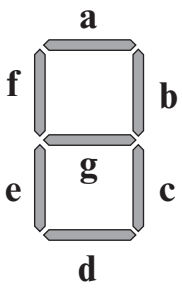
Summing amplifier: $V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots\right)$

Examiner only

Answer **all** *questions.*

1. The diagram shows a 7-segment display.

A logic 1 signal makes a segment light up.



(a) Identify the character generated by the following signals. [1]

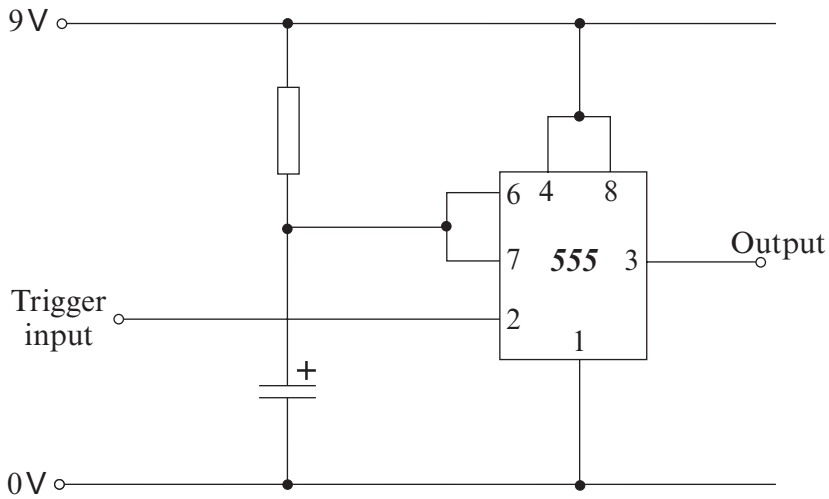
Segments							Character displayed
a	**b**	**c**	**d**	**e**	**f**	**g**	
1	1	1	1	0	0	1	

(b) Complete the signals needed to display the letter 'L'. [1]

Segments							Character displayed
a	**b**	**c**	**d**	**e**	**f**	**g**	
							L

Examiner only

2. *(a)* Select the name of the sub-system shown in the diagram. (Tick (✓) the correct answer.) [1]

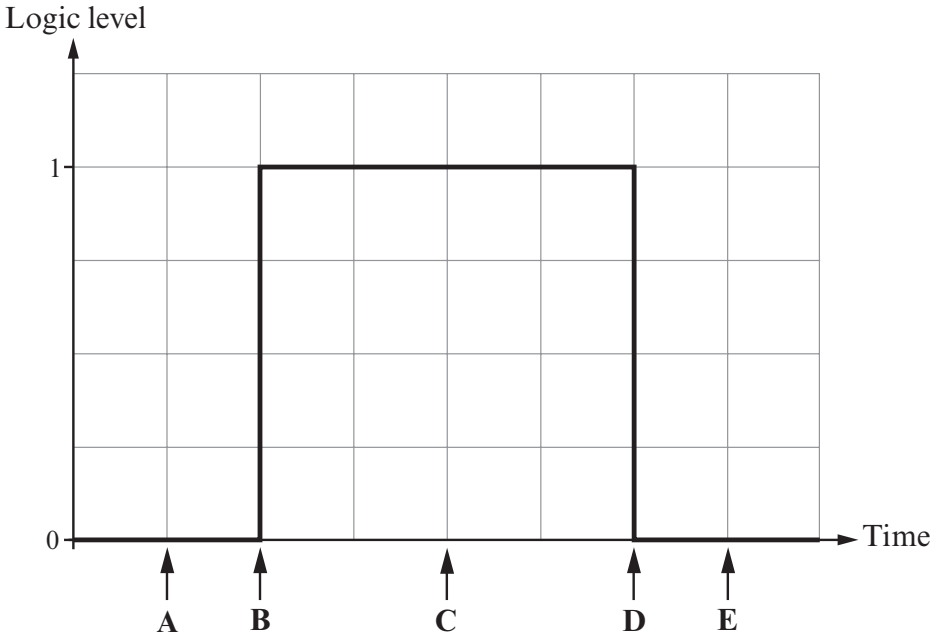


- ☐ Astable
- ☐ Monostable
- ☐ Latch
- ☐ Counter

(b) This sub-system is *falling-edge triggered.*

The pulse shown below is applied to the trigger input.

Select the point **A**, **B**, **C**, **D** or **E** at which the sub-system will be triggered. [1]
(Tick (✓) the correct answer.)



- ☐ **A**
- ☐ **B**
- ☐ **C**
- ☐ **D**
- ☐ **E**

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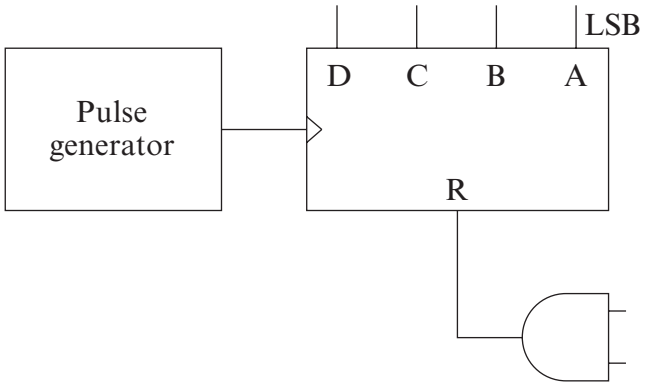
3. A system counts up to 5 and then resets on the 6th pulse.

Output A is the least significant bit (LSB).



(a) What is the output when the count equals 5? [1]

	D	C	B	A
Output				

(b) Select the **two** counter outputs which must be connected to the AND gate to make the counter reset every sixth pulse. (Tick (✓) the correct answers.) [2]

D ☐ C ☐ B ☐ A ☐

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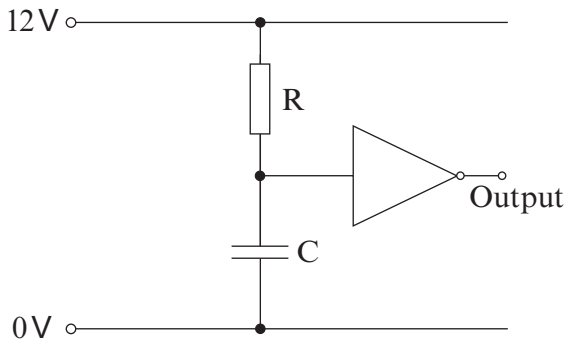
4. The circuit diagram shows an **RC network** connected to an inverting buffer to create a time delay.



(a) Which combination gives the **shortest** time delay? (Tick (✓) the correct answer.) [1]

	Resistor R	Capacitor C
☐	5.6 kΩ	10 µF
☐	560 kΩ	10 µF
☐	5.6 kΩ	100 µF
☐	560 kΩ	100 µF

(b) The buffer inverts the signal from the RC network.

Select the **other** function of the buffer in this circuit. (Tick (✓) the correct answer.) [1]

☐ It acts as a NOT gate.

☐ It ensures that the maximum possible current is taken from the RC network.

☐ It ensures that the time delay is not affected by the current taken by the load.

☐ It reduces the time delay produced by the RC network.

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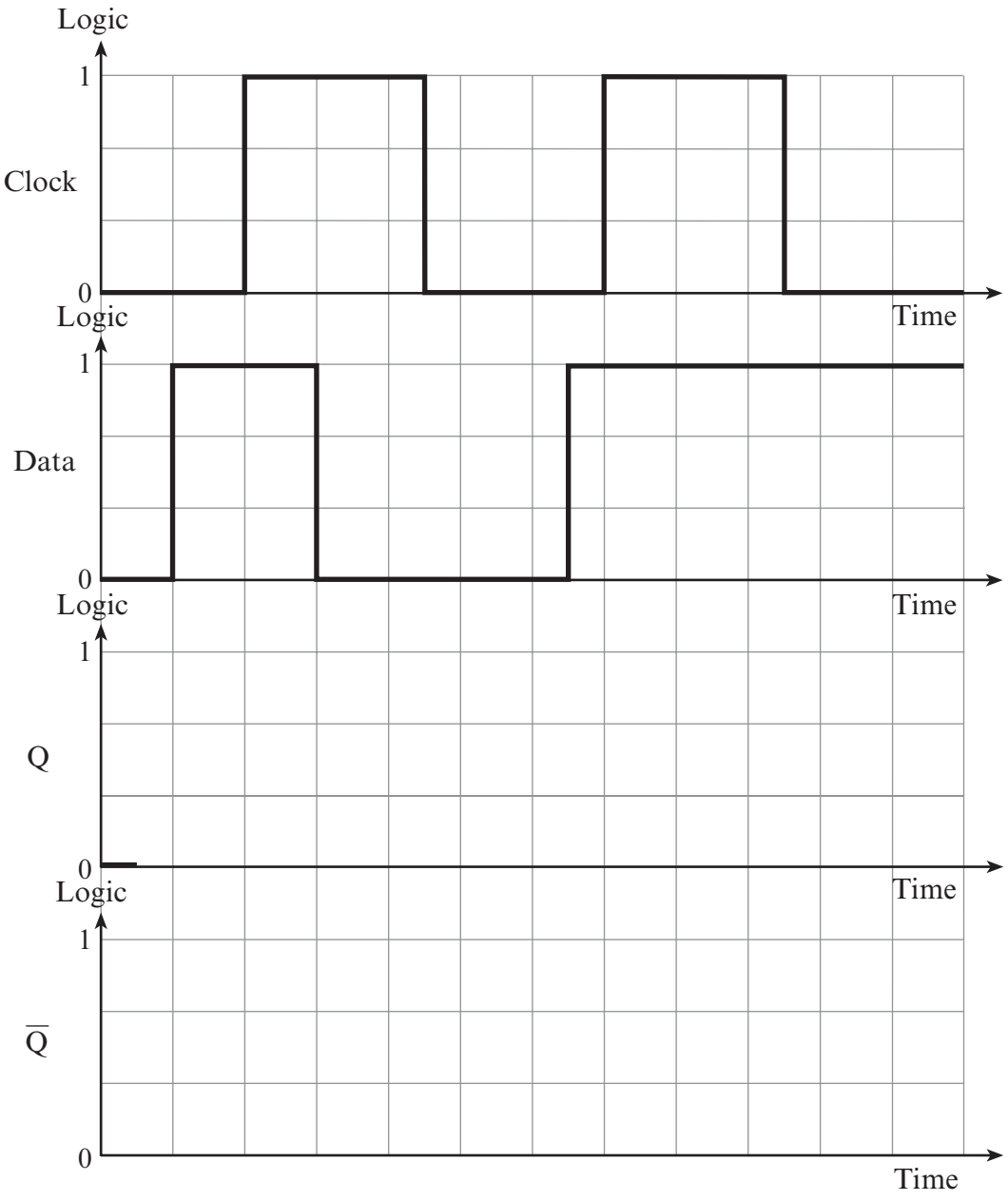
5. A *rising-edge triggered* D-type flip-flop is used in data transfer.

Complete the graphs to show the Q and $\overline{Q}$ outputs. [3]



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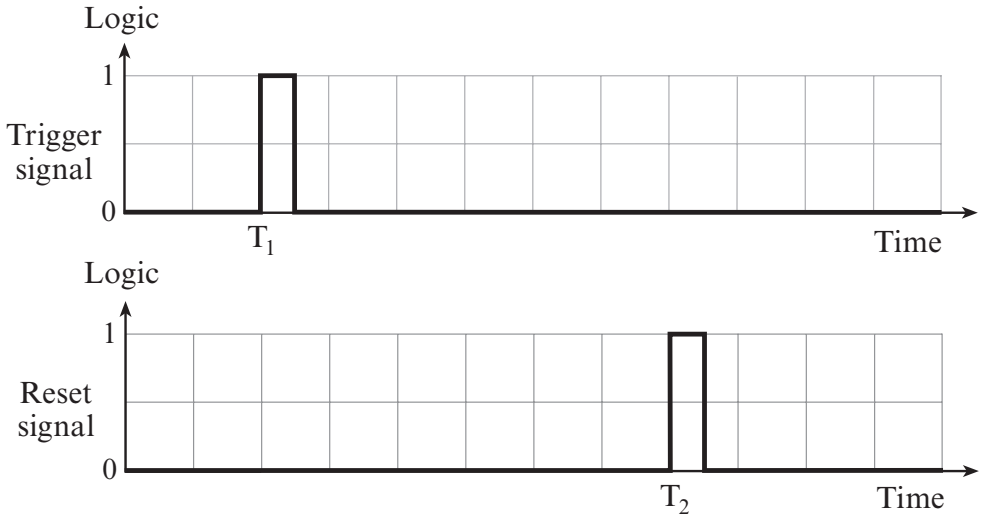
Turn over.

Examiner only

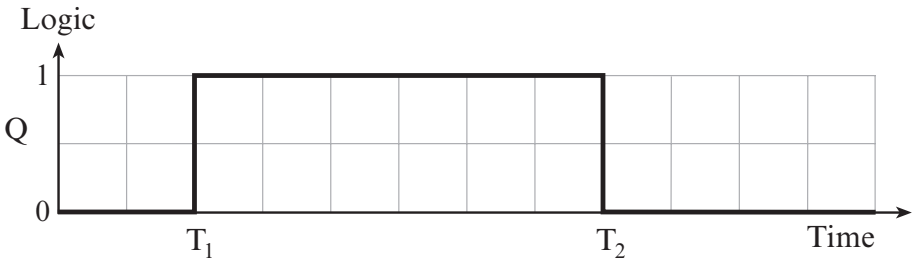
6. A latch sub-system is triggered at time T_1 and reset at time T_2.

The graphs below show the signal that triggers the latch and the reset signal.

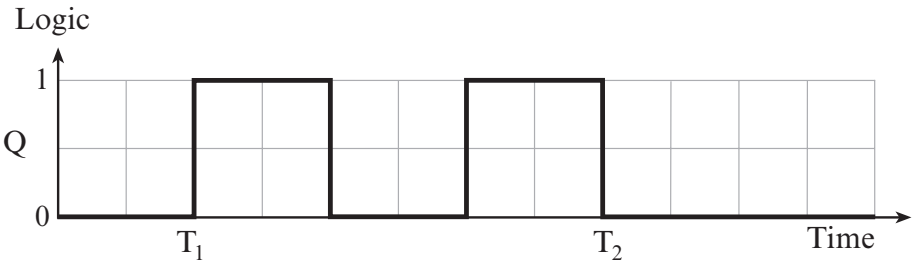


Select the graph that shows the behaviour of the Q output of the latch during this period. [1]
(Tick (✓) the correct answer.)

☐



☐



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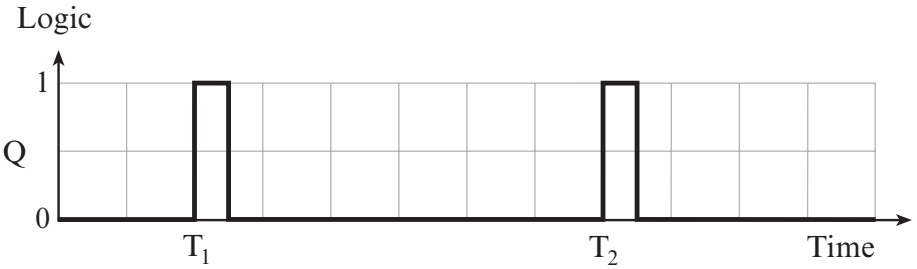
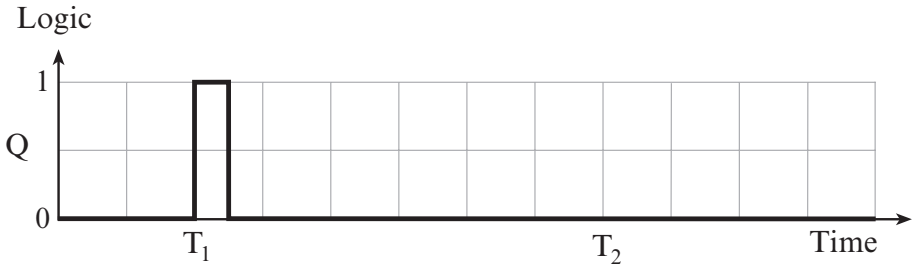


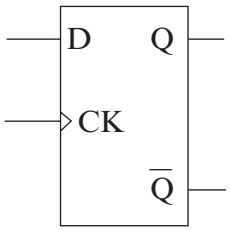
☐



Examiner only

7. A D-type flip-flop will be set up as a one-bit counter.

Part of the circuit diagram is shown opposite:



Select the **two** connections needed to complete the one-bit counter.
(Tick (✓) the correct answers.) [2]

- ☐ The clock input is connected to the pulse source.
- ☐ The data input is connected to the pulse source.
- ☐ The clock input is connected to the Q output.
- ☐ The data input is connected to the Q output.
- ☐ The clock input is connected to the $\overline{Q}$ output.
- ☐ The data input is connected to the $\overline{Q}$ output.

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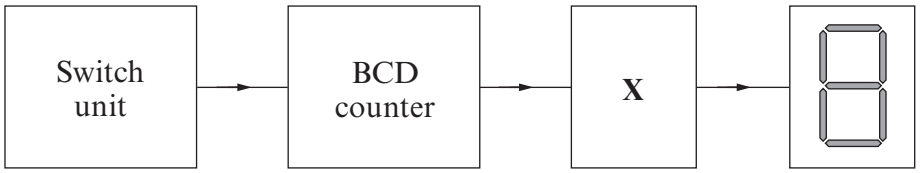
Turn over.

Examiner only

8. Here is the block diagram for a single digit decimal counting system.



(a) Choose the best sub-system for block **X** from the following list: [1]
(Tick (✓) the correct answer.)

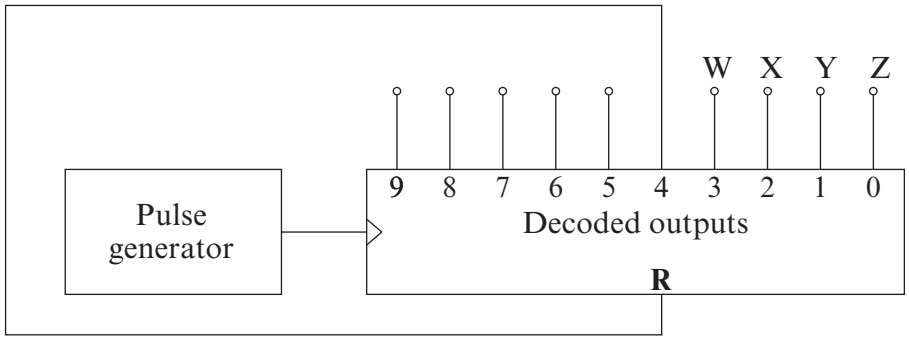
- ☐ monostable
- ☐ transducer driver
- ☐ latch
- ☐ decoder / driver

(b) Which of the following statements is true about 4-bit BCD counters? [1]
(Tick (✓) the correct answer.)

- ☐ The highest decimal number that can be produced is 15.
- ☐ In a decimal counting system, an OR gate must be used to reset it.
- ☐ It cannot be used to count pulses from mechanical switches.
- ☐ The highest binary number that can be produced is 1001.

Examiner only

9. The diagram shows part of a lighting sequence, controlled by a decade counter. W, X, Y and Z are connected to LEDs.



Reset input **R** is *active-high*, so the counter resets when **R** receives a logic 1 signal.

Complete the table by writing either '**On**' or '**Off**' to show the state of the LEDs as the sequence progresses. [2]

Pulse	LEDs			
	Z	Y	X	W
0	On	Off	Off	Off
1				
2				
3				
4				

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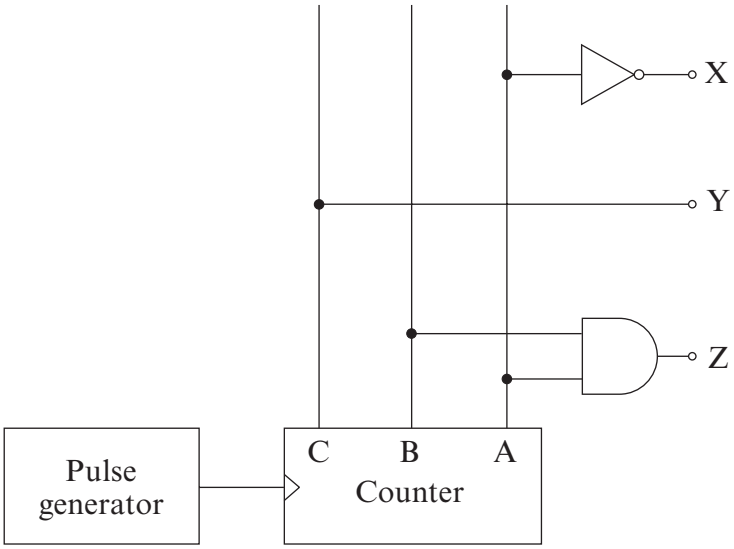
10. The circuit diagram shows part of a lighting controller.



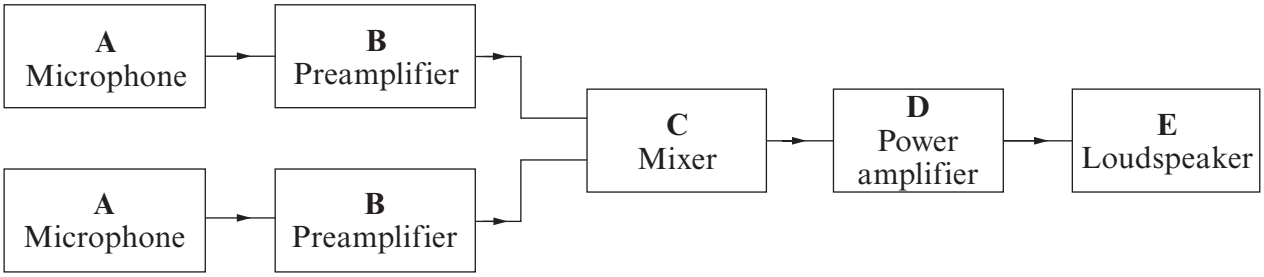
Complete the table by adding:

- either "**1**" or "**0**" in each box of the X, Y and Z columns; [3]
- either "**1**" or "**0**" in the last row of columns C, B and A (for pulse 6). [1]

Pulses from pulse generator	**Counter outputs**			**X**	**Y**	**Z**
	C	**B**	**A**			
0	0	0	0			
1	0	0	1			
2	0	1	0			
3	0	1	1			
4	1	0	0			
5	1	0	1			
6						

Examiner only

11. The block diagram represents a typical amplifier system.
It uses five different sub-systems, labelled **A** to **E**.



Select the blocks designed to:

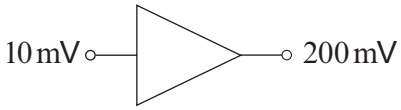
(a) boost the current delivered to the sub-system that follows it; [1]

Answer .....

(b) boost the signal voltage obtained from the previous sub-system. [1]

Answer .....

12. A voltage amplifier produces an output signal with amplitude 200 mV when the input signal has an amplitude of 10 mV.

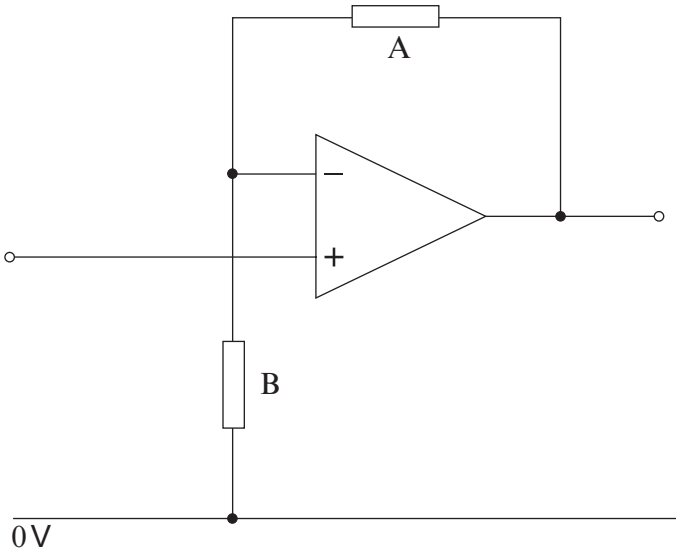


(a) What is the voltage gain of the amplifier? [1]

Answer .....

(b) Select the pair of resistors that would give the non-inverting amplifier a voltage gain of 12. (Tick (✓) the correct answer.) [1]

	Resistor A	Resistor B
☐	1 kΩ	11 kΩ
☐	11 kΩ	1 kΩ
☐	12 kΩ	1 kΩ
☐	1 kΩ	12 kΩ



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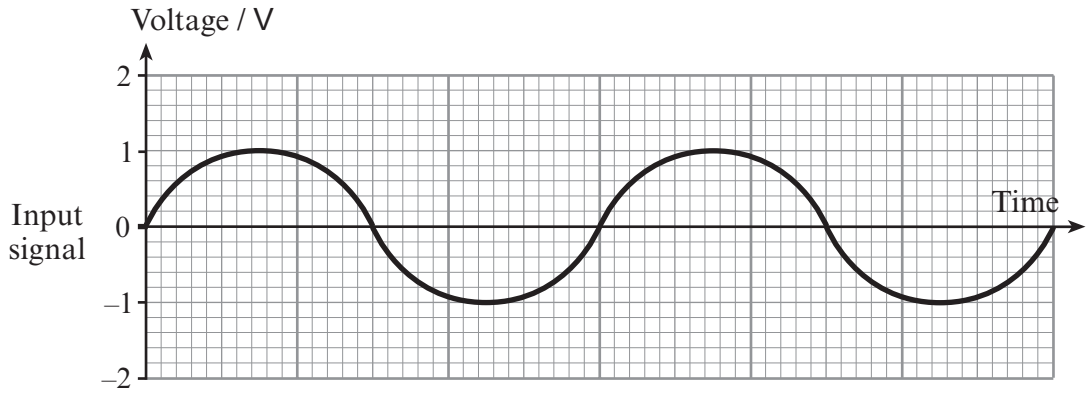
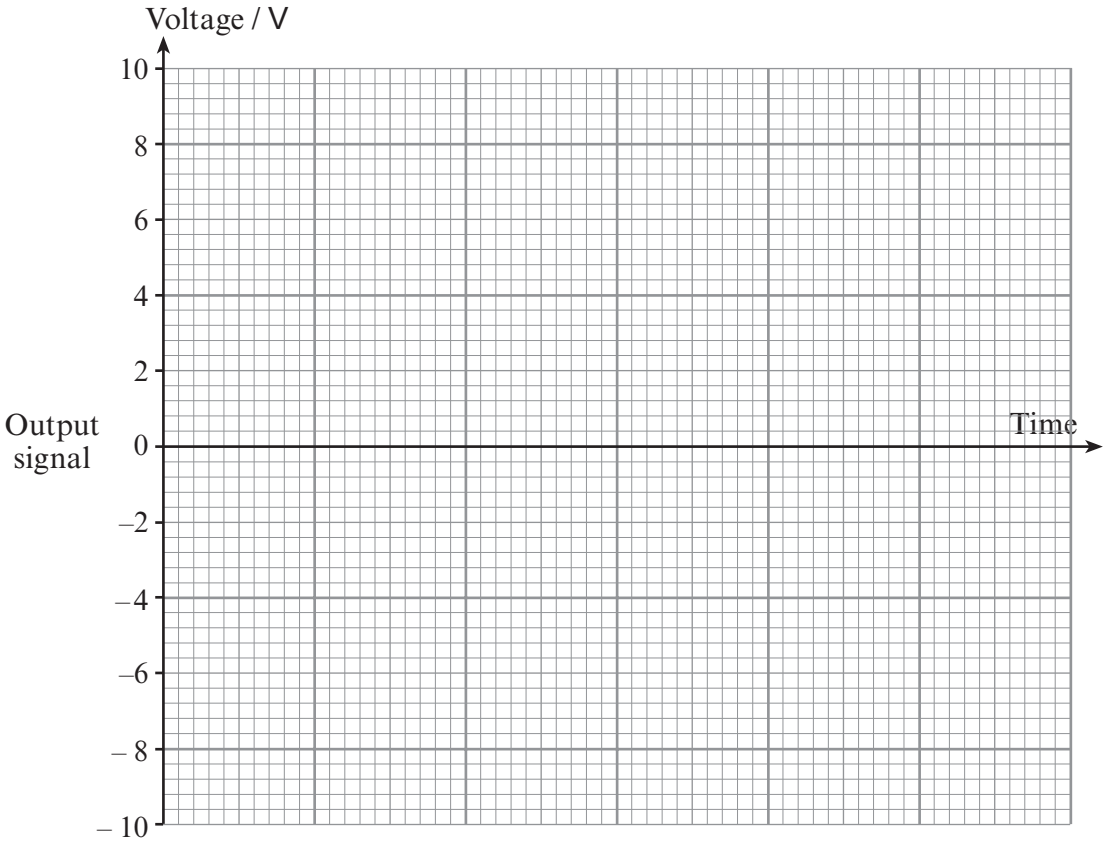
13. A non-inverting amplifier has a voltage gain of 8.

The upper graph shows the signal applied to the input of the amplifier.

Draw the corresponding output signal. [1]





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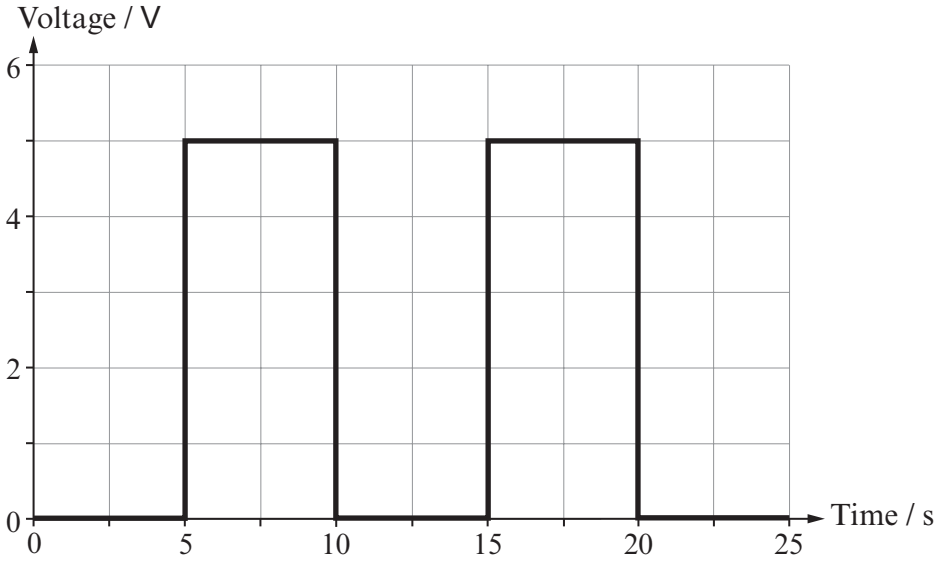
14.



For the signal shown, what is:

(a) the amplitude? (Tick (✓) the correct answer.) [1]

- ☐ 10 V
- ☐ 5 V
- ☐ 5 s
- ☐ 10 s

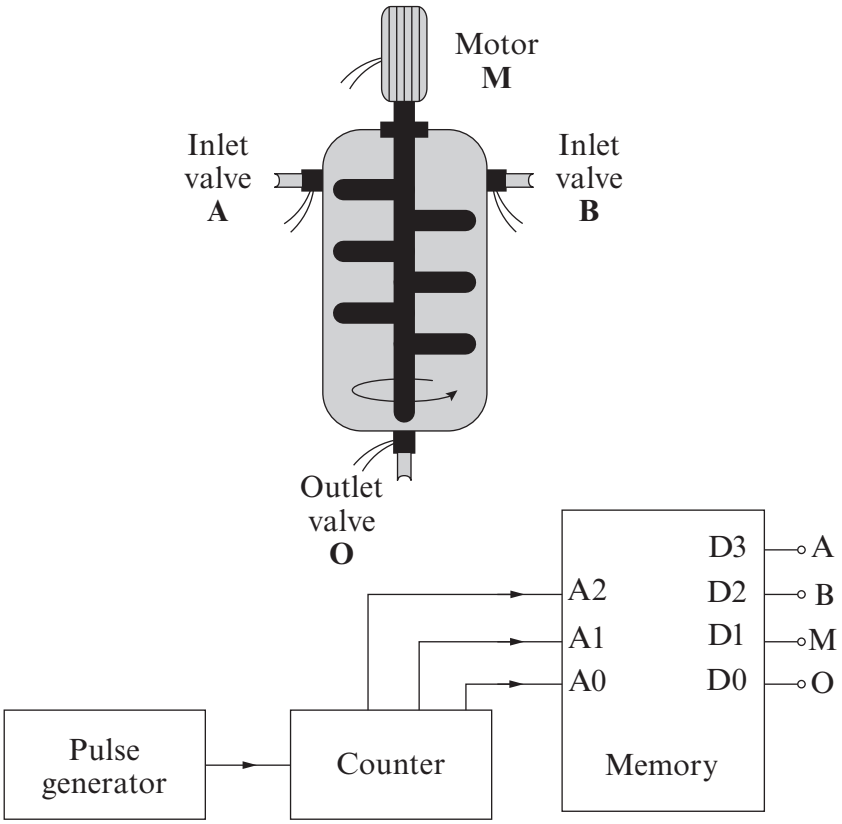
(b) the period? (Tick (✓) the correct answer.) [1]

- ☐ 10 V
- ☐ 5 V
- ☐ 5 s
- ☐ 10 s

(c) the frequency? [1]

Answer ..... Hz

15. A motor-driven paddle is used to mix paint. The valves are normally closed. Liquids enter through inlet valves **A** and **B**, and are mixed before leaving through outlet valve **O**.
The system is controlled by data stored in a memory IC.
The valves and motor operate on a logic 1 signal.
The data stored in part of the memory is given below.



A2	A1	A0	D3	D2	D1	D0
0	0	0	0	0	1	0
0	0	1	1	1	1	0
0	1	0	0	1	1	0
0	1	1	0	0	0	0
1	0	0	0	0	1	1
1	0	1	0	0	0	1
1	1	0	0	0	1	1
1	1	1	Reset			

Examiner only

(a) The counter is reset before each mixing cycle. Describe the stages of the process between counter reset and the outlet valve opening. *(No timing information is needed.)* [2]

.....

.....

.....

.....

(b) The pulse generator outputs pulses with a period of 2 s.

For how long is the outlet valve open in each mixing cycle? [1]

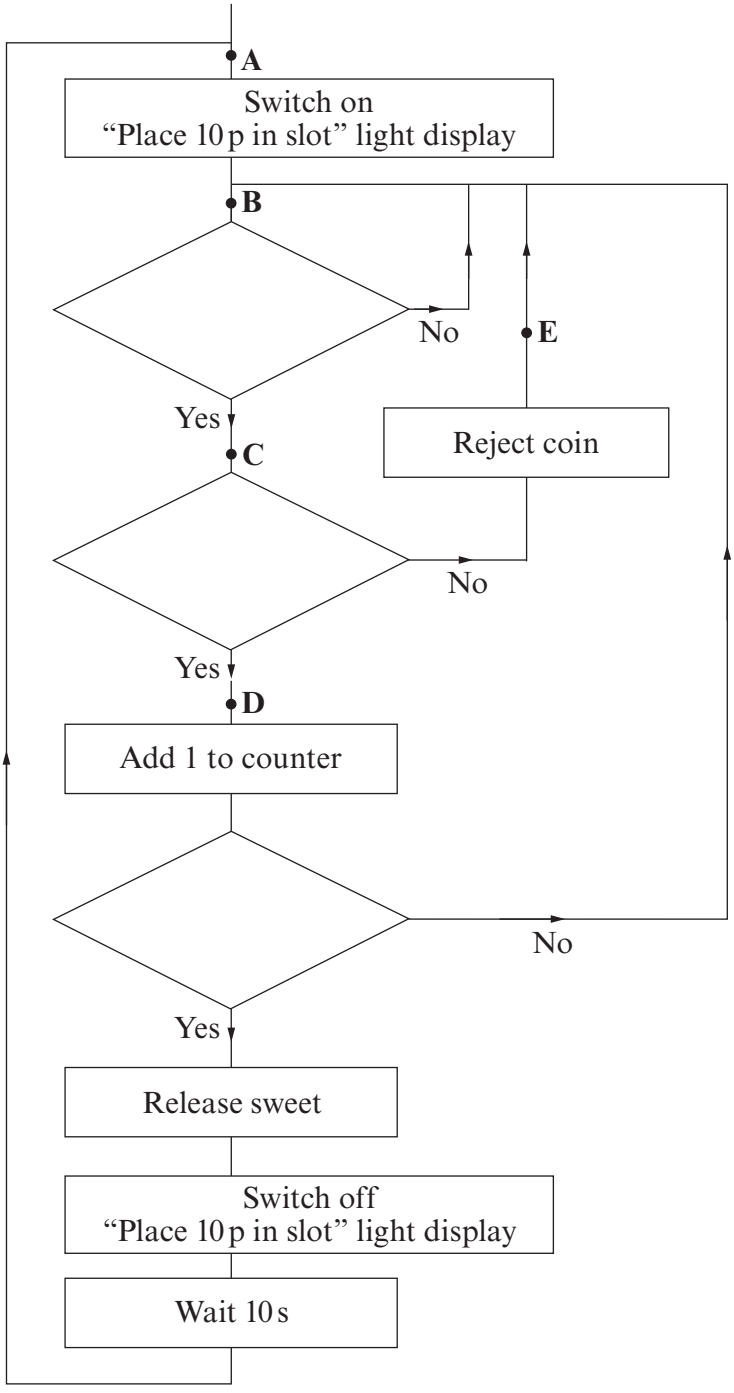
Answer ..... s

(c) The memory IC used for this task has three address bits.

How many address locations are there in this memory IC? [1]

Answer .....

16. Here is part of the flowchart for a dispensing machine for sweets.



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(a) Add the following labels to the correct boxes:

- "Is it 10 p?"
- "Counter = 5?"
- "Coin detected?"

[3]

(b) How much does a sweet cost? [1]

Answer ..... p

(c) At which point in the flowchart, **A**, **B**, **C**, **D** or **E**, should the instruction "Reset the counter" be added? [1]

Answer .....

Examiner only

17. *(a)* A comparator can be used as an interface between a light sensor and a digital system. Here are four statements about the comparator used in this way.
Select the correct **one**. (Tick (✓) the correct answer.) [1]

☐ It has a single switching threshold fixed at 0.7 V.

☐ It has a single switching threshold at a voltage which can be varied.

☐ It has two fixed switching thresholds.

☐ It has two switching thresholds at voltages which can be varied.

(b) Usually, it is better to use a Schmitt inverter.
Which statement gives the benefit of the Schmitt inverter over the comparator in this application? (Tick (✓) the correct answer.) [1]

☐ It stops contact bounce in the light sensor.

☐ It stops rapid output switching when the light level fluctuates slightly.

☐ It improves the rise-time of the signal.

☐ It boosts the current to the output device.

18. In a 555 monostable circuit, the time delay T is given by the formula:

$$T = 1.1\,RC$$

Calculate the time delay produced when:

$R = 1\ M\Omega.$
$C = 10\ \mu F.$ [1]

.....

.....

Answer ..... s

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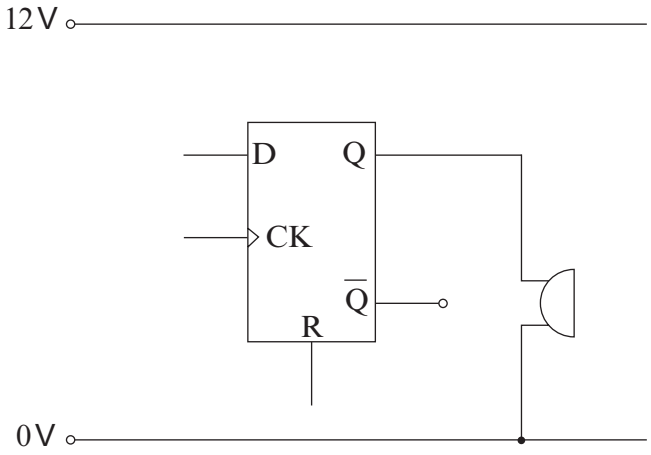
19. Here is an incomplete circuit diagram for a latch.



(a) The D-input must be connected to:

☐ the clock input;

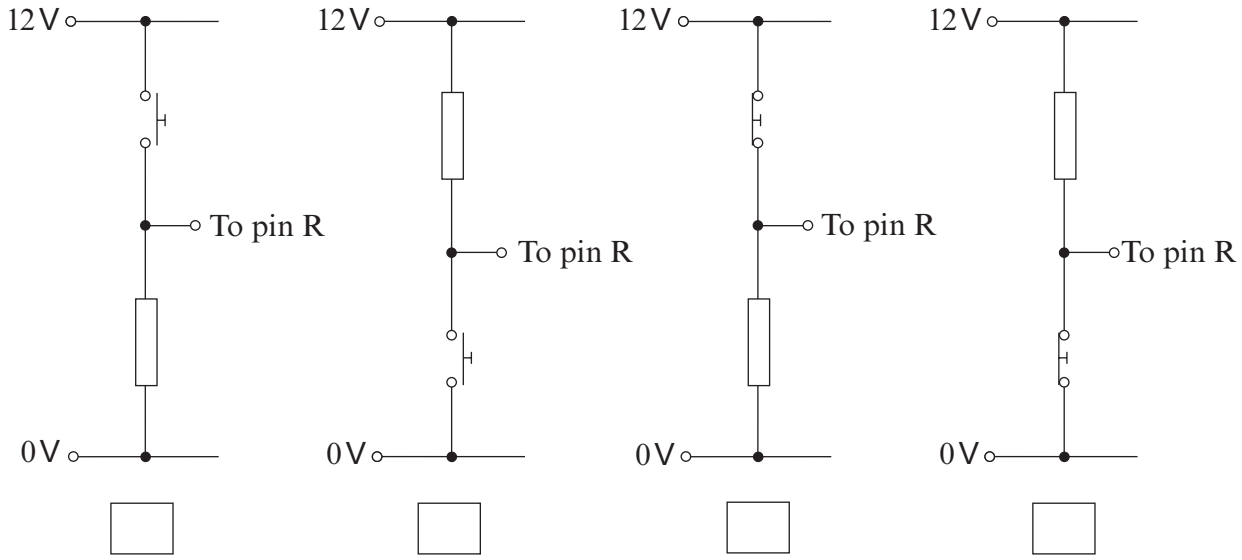
☐ the $\overline{Q}$ output;

☐ the 12 V power rail;

☐ the 0 V power rail. [1]

(b) The latch resets when pin R receives a logic 1 signal.

Which **two** switch units will reset the latch when the switch is pressed?
(Tick (✓) the correct answers.) [2]

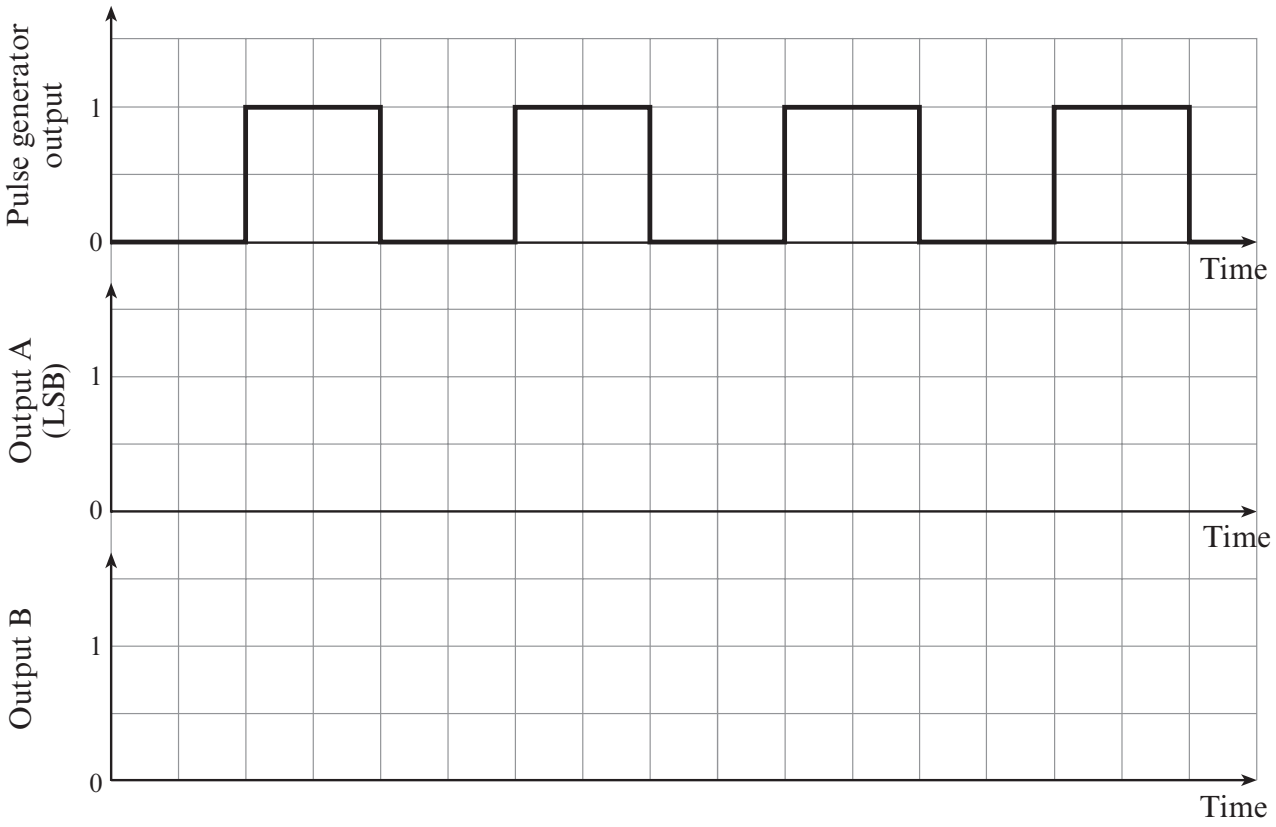


Examiner only

20. A *rising-edge triggered* 2-bit up counter is connected to a pulse generator. Output A is the least-significant bit (LSB). Initially, it is reset.

The top graph shows the pulses received from the pulse generator.

Draw the resulting signals at the outputs. [3]



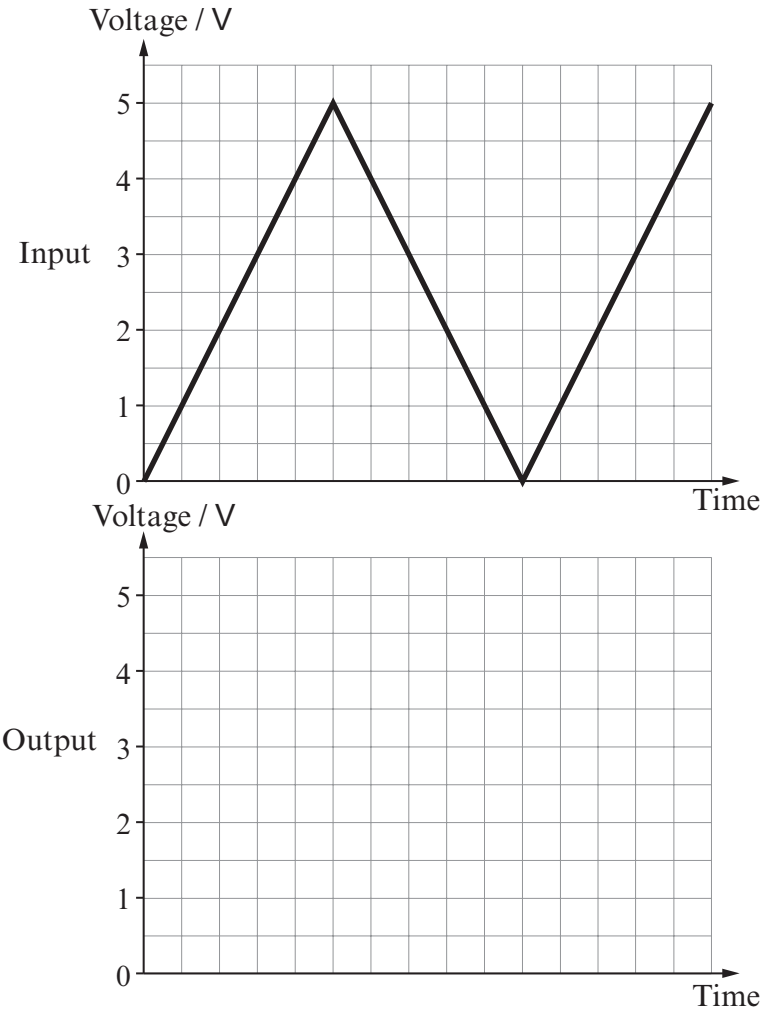
Examiner only

21. The following data sheet provides information about a Schmitt Inverter:

> When connected to a 5 V power supply:
> - Logic 0 = 0 V
> - Logic 1 = 5 V
> - The output changes from logic 1 to logic 0 when a **rising** input voltage reaches 3 V
> - The output changes from logic 0 to logic 1 when a **falling** input voltage reaches 1 V

An engineer tests it by applying the signal shown in the upper graph to the input.

Draw the expected output signal. [4]



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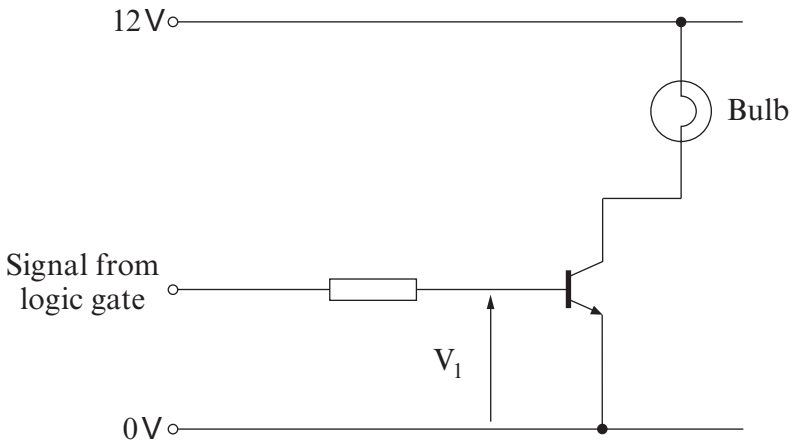
22. The circuit diagram for the interface to a bulb is shown below.



(a) The signal from the logic gate switches from 0.5 V (logic 0) to 8.0 V (logic 1).

Complete the table to show the corresponding values of voltage V_1. [2]

Logic gate output	V_1
0.5 V	 V
8.0 V	 V

(b) The bulb in the lamp unit is rated at 12 V, 100 mA.

The transistor has a current gain (h_{FE}) of 50.

Calculate the base current when the transistor is just saturated. [1]

Answer ..... mA

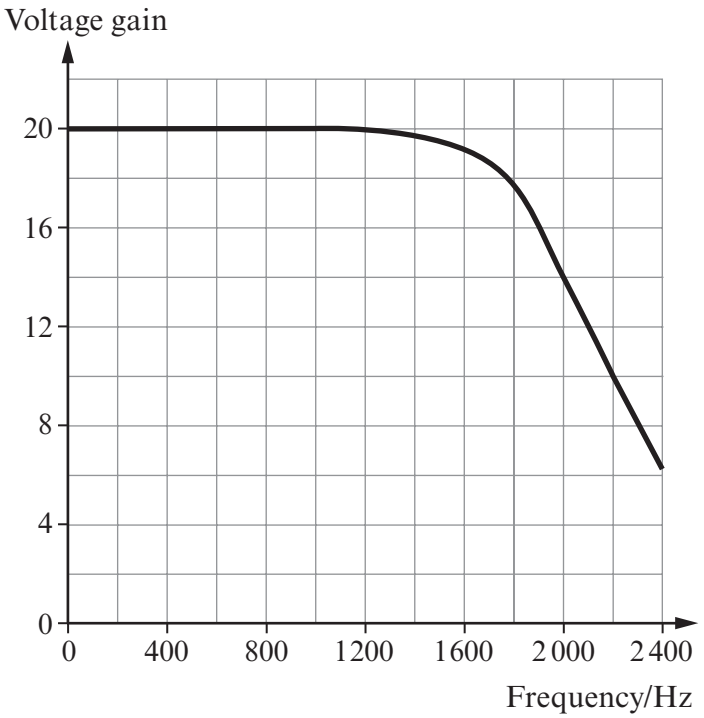
Examiner only

23. The output signal of an amplifier is clipped.

What is the reason for this? (Tick (✓) the correct answer.) [1]

- ☐ The amplitude of the input signal is too big for the power supply.
- ☐ The frequency of the output signal exceeds the bandwidth of the amplifier.
- ☐ The voltage gain formula does not apply to digital signals.
- ☐ The output signal is not inverted.

24. The graph shows the effect of changing the signal frequency on an amplifier's voltage gain.



What is the bandwidth of the amplifier? (Tick (✓) the correct answer.) [1]

- ☐ 1000 Hz
- ☐ 2000 Hz
- ☐ 2200 Hz
- ☐ 2400 Hz

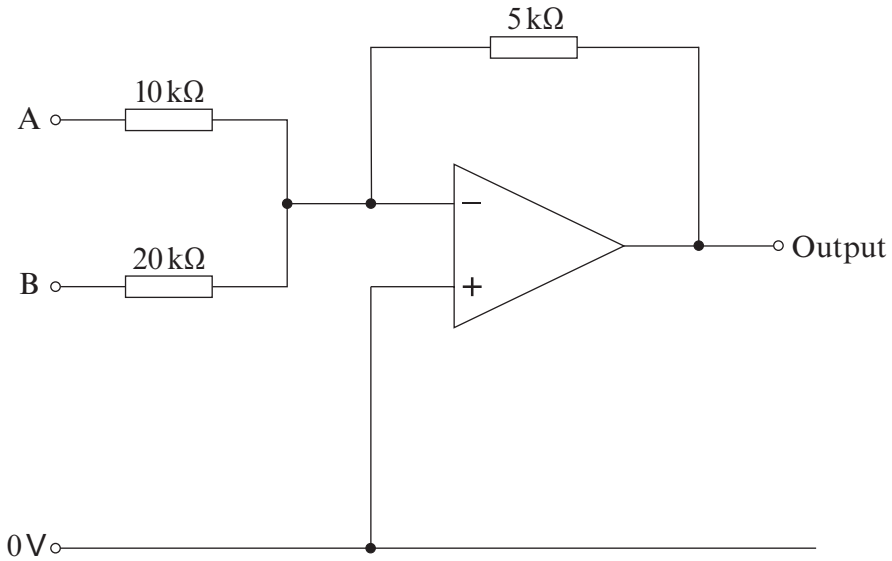
TURN OVER FOR THE LAST QUESTION

Examiner only

25. Audio mixers are used to combine signals from a number of different sources.

The mixer in the diagram is tested by applying the following signals.

Input A = 1.0 V
Input B = 2.0 V



(a) Which **one** of the following shows the correct formula and values to calculate the output voltage? (Tick (✓) the correct answer.) [1]

☐ $V_{OUT} = -20\left(\frac{1}{10} + \frac{2}{5}\right)$

☐ $V_{OUT} = -10\left(\frac{1}{20} + \frac{2}{5}\right)$

☐ $V_{OUT} = -5\left(\frac{1}{20} + \frac{2}{10}\right)$

☐ $V_{OUT} = -5\left(\frac{1}{10} + \frac{2}{20}\right)$

(b) Calculate the output voltage. [1]

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Answer V

END OF PAPER