GCSE MARKING SCHEME

SUMMER 2017

ELECTRONICS - E1
4161/01

INTRODUCTION

This marking scheme was used by WJEC for the 2017 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

GCSE ELECTRONICS - E1

Summer 2017 March scheme

1. (a) Buzzer [1]

Lamp [1]

Push to break [1]

(b) [3]

Input sub-system	Processing sub-system	Output sub-system
Sound sensing unit	NOT gate	Motor unit
Magnetic switch unit	Delay unit	Lamp unit
Pulse generator	Latch unit	
	Comparator	

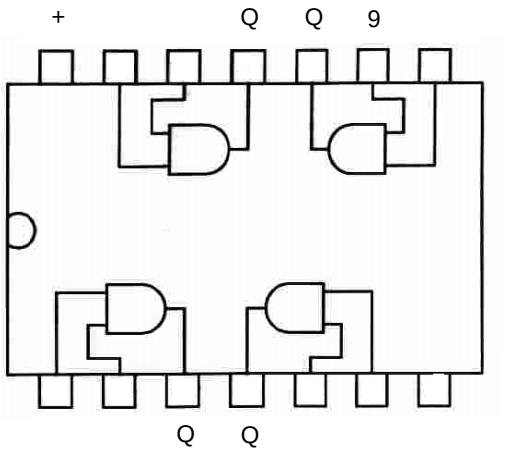
2. (a) 4 V [1]

(b) 5 mA [1]

(c) 4 V [1]

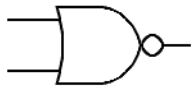
(d) 3 mA [1]

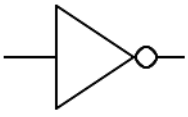
3. (a)-(c) [3]



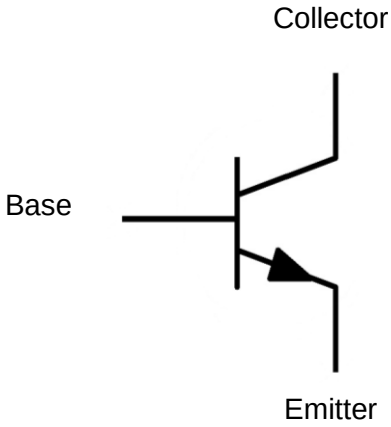
(d) AND gate [1]

4. [2]

NOR gate 

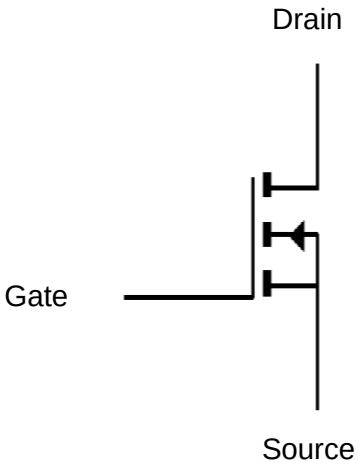
NOT gate 

5. (a)



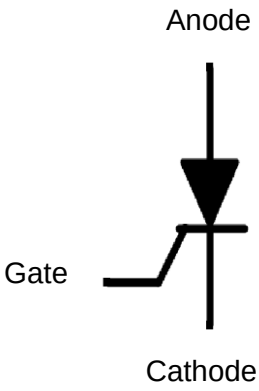
[1]

(b)



[1]

(c)



[1]

6. Band 1 – Green [1]

Band 2 – Blue [1]

Band 3 – Black [1]

7. (a) $P = 6 \times 15$ [1]

(b) 90 W [1]

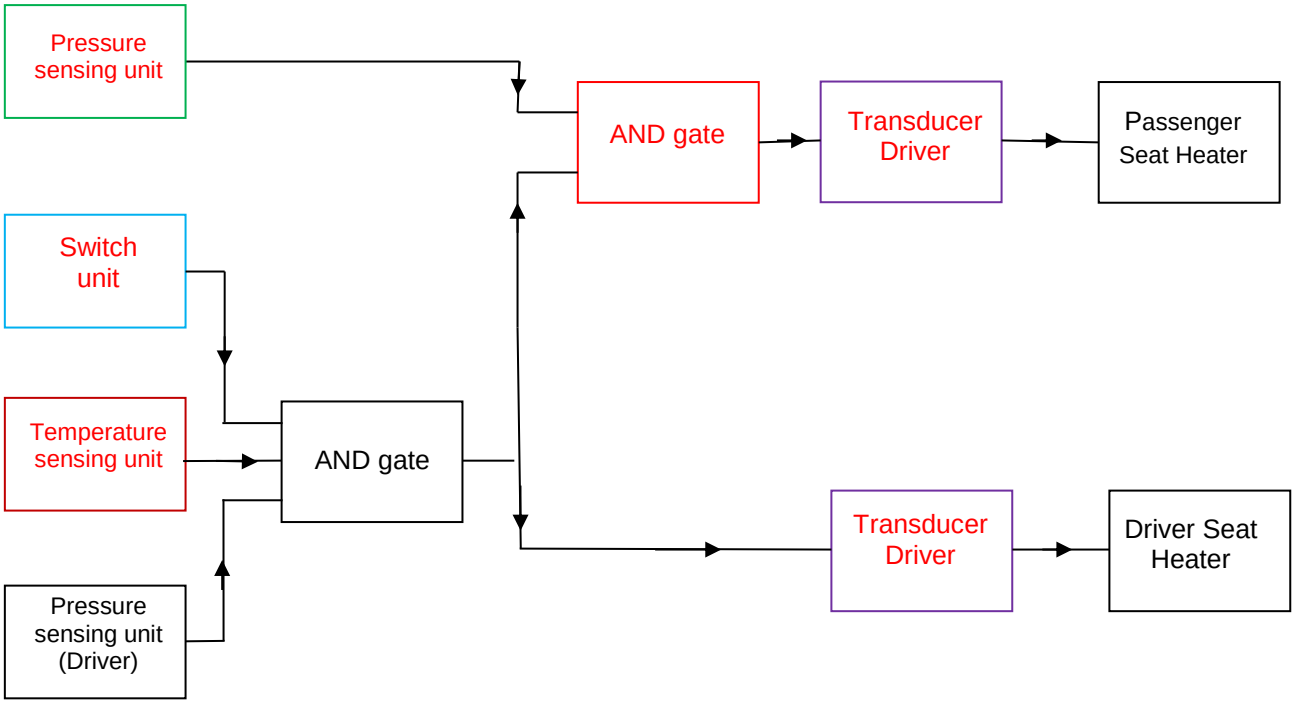
8. (a) Variable resistor [1]

(b) 9 V [1]

(c) (i) The resistance of component Y would increase [1]

(ii) V_{OUT} would increase [1]

9. [5]

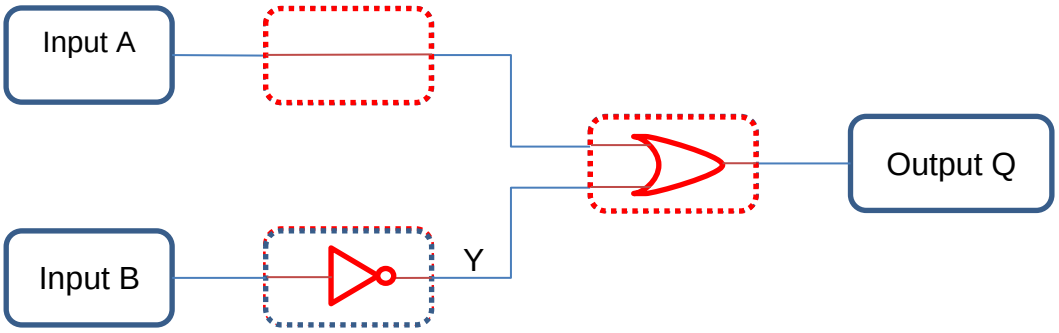


1 Mark for each of Pressure sensing unit, Switch Unit, Temperature sensing unit, AND Gate,
1 Mark for 2 x Transducer driver.
Switch Unit / Temperature sensor are interchangable.

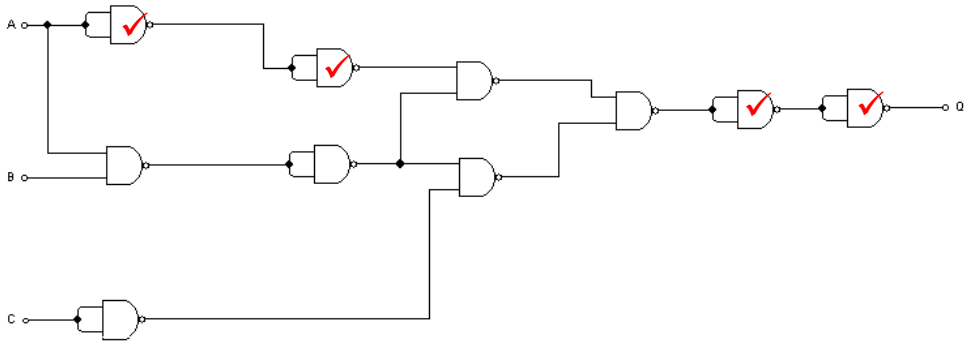
10. (a) OR gate [1]

(b) AND gate [1]

11. [3]



12. [2]



13. 32.1 kΩ, 28 kΩ & 2.93 kΩ [3]

14. (a) [1]

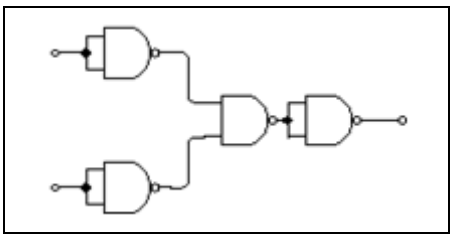
Inputs		Output
A	B	Q
0	0	0
0	1	0
1	0	1
1	1	0

(b) [1]

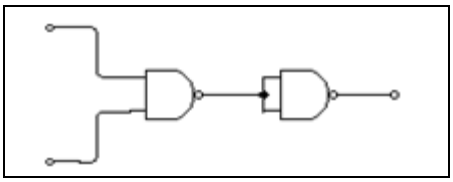
Inputs		Output
A	B	Q
0	0	1
0	1	1
1	0	0
1	1	1

15. [3]

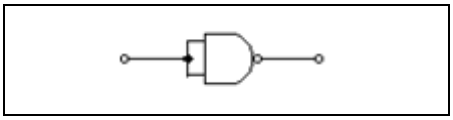
NOR gate



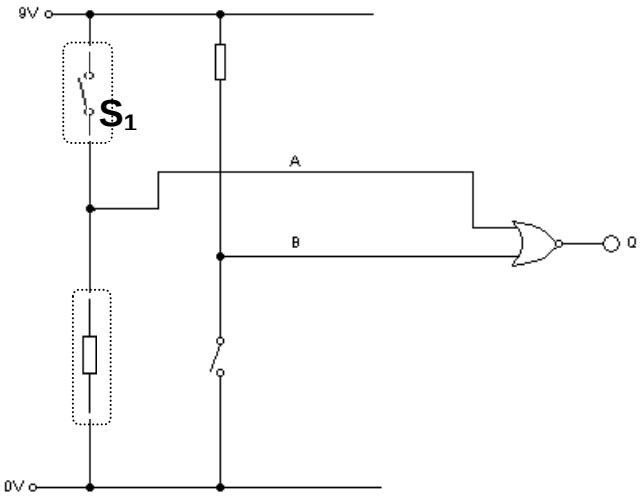
AND Gate



NOT gate



16. (a) [1]



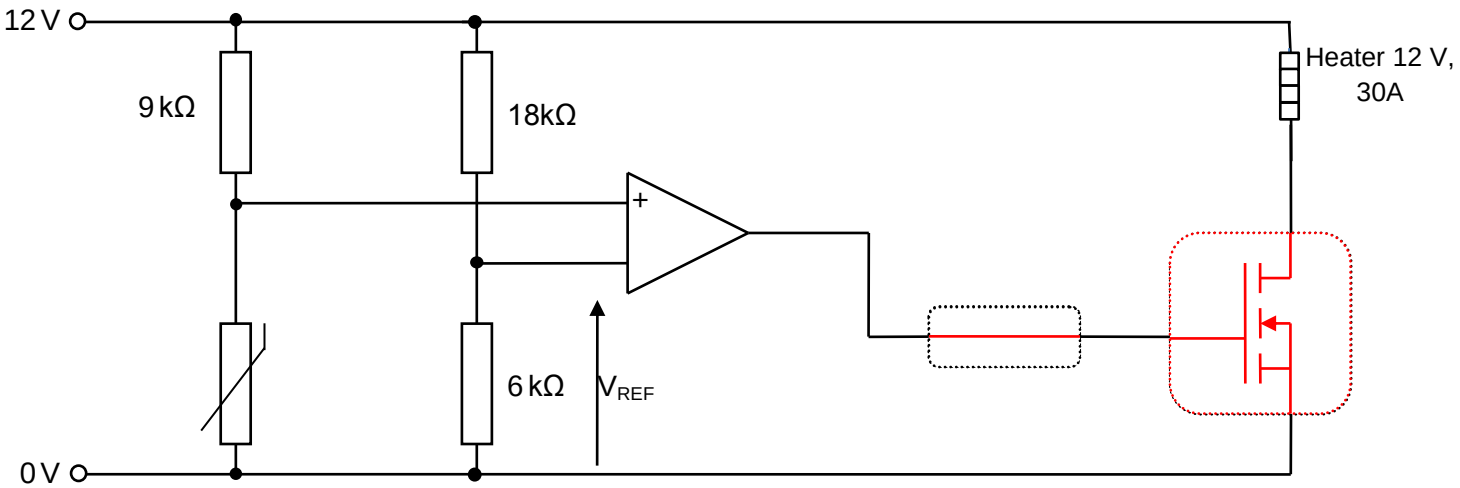
(b) Pull up resistor ensures input B at logic 1 when S_2 open [1]

(c) S1 open & S2 closed [1]

17. (a) $V_{REF} = \frac{6}{6+18} \times 12$ [1]

(b) 3 V [1]

(c) [2]



(d) Make any one of the fixed resistors variable / Replace a fixed resistor with a variable. Do not accept: A variable resistor which is unqualified as to where it is used.

[1]

18. (a) 7 V [1]

(b) $R = \frac{7}{25}$ [1]

(c) 0.28 kΩ [1]

(d) 300 Ω (e.c.f. from (c)) [1]