GCSE MARKING SCHEME

SUMMER 2018

ELECTRONICS - E1
4161/01

INTRODUCTION

This marking scheme was used by WJEC for the 2018 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

1a. Transistor
Diode
Push to make switch

3 x 1 mark

1b.

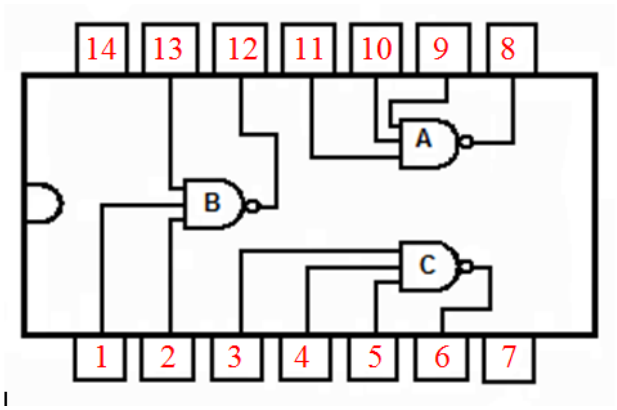
Input sub-systems	Processing sub-systems	Output sub-systems
Temperature sensing unit	OR gate	Buzzer unit
Switch Unit	Delay unit	Solenoid unit
Light sensing unit	Transistor switch unit	Lamp unit

1 mark per correct column – Max 3

2a. 6V
2b. 5mA
2c. 3V
2d. 7mA

4 x 1 mark

3a.



All pins correct = 1 mark

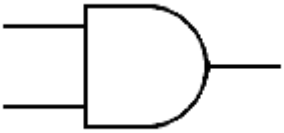
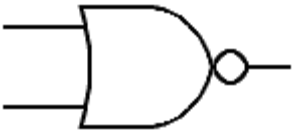
3b. Pins 1, 2 and 13 identified (e.c.f for incorrect labelling of pins)

1 mark

3c. Pin 8 **Only** identified (e.c.f for incorrect labelling of pins).

1 mark

4.

Logic Symbol	Symbol
AND gate	
NOR gate	

1 mark for each correct symbol

5. Middle diagram ticked only

1 mark

6. Band 1 – 3, Band 2 = 9, Band 3 = 00

3 x 1 mark = Max 3

7a. P = 25 x 8

1 mark

7b. 200W

1 mark

8a. LDR

1 mark

8b. 8V

1 mark

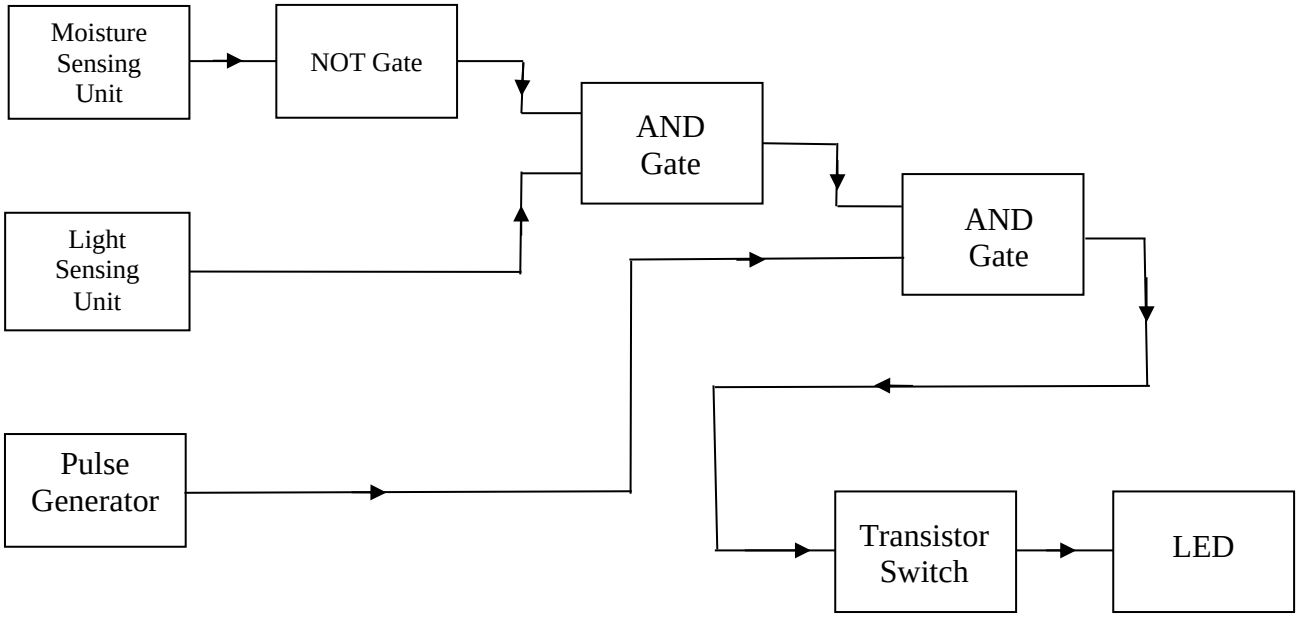
8c. V_Y would increase.

1 mark

8d. Light level falling on (increase of resistance of) LDR causes decrease in V_Y

1 mark

9.



6 x 1 mark for each correct box

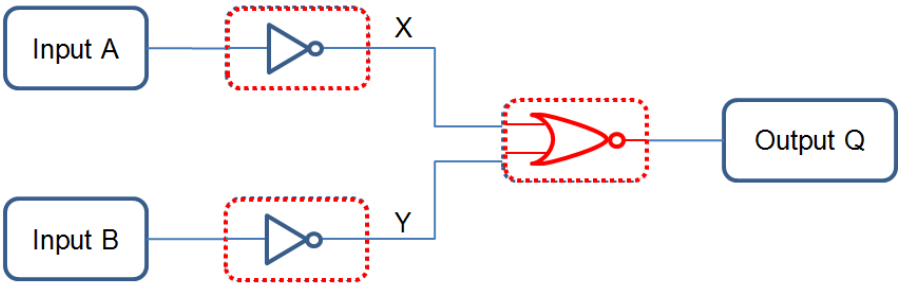
10a. NAND gate

1 mark

10b. OR gate

1 mark

11a.

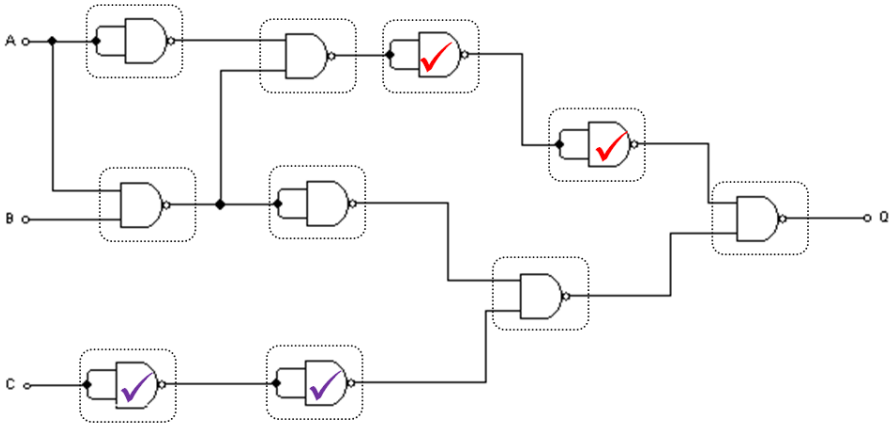


1 mark for each correct gate inserted = 3 Max.

11b. AND gate.

1 mark

12.



1 mark for each correct pair of gates, -1 for each additional tick over 4 = 2 Max

13. 49.7kΩ
34kΩ
3kΩ

3 x 1 mark

14a. Bottom right table.

Inputs		Output
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

☑

1 mark

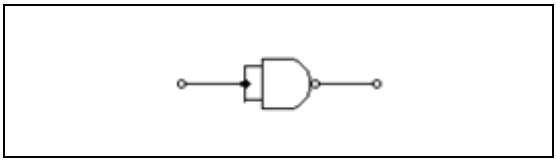
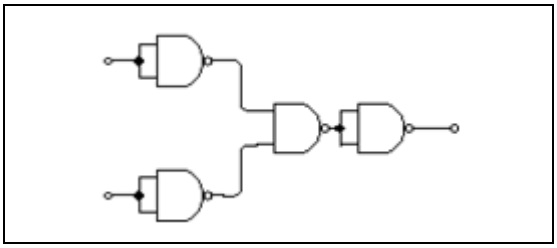
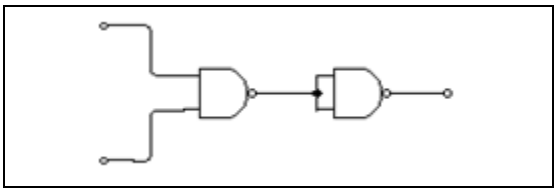
14b. Top left table

Inputs		Output
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

☑

1 mark

15.

Standard Gate	NAND Equivalent Circuit
NOT gate	
NOR Gate	
AND gate	

3 x 1 mark

16a. Bottom left formula - $V_{OUT} = \frac{4.7}{6.8 + 4.7} \times 10$

1 mark

16b. 4.086V (accept 4.08 – 4.10)

1 mark

16c. Output voltage is continuously variable.

1 mark

Output voltage covers full range of input voltage.

1 mark

17a. 12k top RHS, 3k bottom RHS — 2 marks or
3k top RHS, 12k bottom RHS — 1 mark

17b. Thermistor on bottom of LHS,

1 mark

Any resistor in top.

1 mark

17c. Change any fixed resistor to a variable resistor (Do not accept – use a variable resistor)

1 mark

18a. 4V

1 mark

18b. $R = \frac{4}{25}$

1 mark

18c. 0.16kΩ

1 mark

18d. 180Ω

1 mark